HYBRID DIGITAL/RF ENVELOPE PREDISTORTION LINEARIZATION FOR HIGH POWER AMPLIFIERS IN WIRELESS COMMUNICATION SYSTEMS

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Wangmyong Woo

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Approved by:

Dr. J. Stevenson Kenney, Advisor
School of Electrical & Computer Engineering
Georgia Institute of Technology

Dr. Mary A. Ingram
School of Electrical & Computer Engineering
Georgia Institute of Technology

Dr. G. Tong Zhou
School of Electrical & Computer Engineering
Georgia Institute of Technology

Dr. Vikram Krishnamurthy
VT Silicon, Inc.

Dr. Robert K. Feeney
School of Electrical & Computer Engineering
Georgia Institute of Technology

Date Approved: April 12, 2005

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LIST OF ABBREVIATIONS

2G	second generation
3G	third generation
ACPR	adjacent channel power ratio
ADC	analog-to-digital converter
ADS	advanced design system
AGC	automatic gain control
AM	amplitude modulation
APD	analog predistortion
BER	bit-error rate
BW	bandwidth
CDMA	code division multiple access
CFB	Cartesian feedback
CMOS	complementary metal oxide semiconductor
DAC	digital-to-analog converter
dB	decibel
dBc	decibel relative to a carrier level
dBm	decibel relative to a milliwatt
DC	direct current
DCM	digital clock manager
DDI	direct distortion inverse
DMB	digital multimedia broadcast
DPD	digital predistortion
DQPSK	differential quadrature phase shift keying
DSP	digital signal processing
DUT	device under test
EDET	envelope detector
EER	envelope elimination and restoration
EFB	envelope feedback
EPD	envelope predistortion
EVM	error vector magnitude
FB	feedback
FET	field effect transistor
FF	feedforward
FIFO	first-in-first-out
FPGA	field programmable gate array
GHz	giga hertz
GMSK	Gaussian minimum shift keying
GPIB	general-purpose interface bus
HFET	heterostructure field effect transistor
HPA	high-power amplifier
HPA	high-power amplifier

I	in-phase
IC	integrated circuit
IF	intermediate frequency
IMD	intermodulation distortion
IMD3	third order intermodulation distortion
JTAG	joint test access group
kHz	kilo hertz
LDMOS	lateral diffused metal oxide semiconductor
LINC	linear amplification with nonlinear components
LMS	least mean square
LO	local oscillator
LPA	low-power amplifier
LPF	lowpass filter
LSB	least significant bit
LUT	look-up table
MCPA	multicarrier power amplifier
MHz	mega hertz
MMS	multimedia messaging service
MSE	mean squares error
OQPSK	offset quadrature phase shift keying
P_{1dB}	1 dB gain compression point
PA	power amplifier
PAPR	peak to average power ratio
PC	personal computer
PCB	printed circuit board
PD	predistortion
PDF	probability density function
PEP	peak envelope power
PM	phase modulation
PWM	power meter
PSK	phase shift keying
Q	quadrature-phase
QAM	quadrature amplitude modulation
QPSK	quadrature phase shift keying
RAM	random access memory
RF	radio frequency
SA	spectrum analyzer
SCPA	single carrier power amplifier
SG	signal generator
SNDR	signal-to-noise and distortion ratio
SNR	signal-to-noise ratio
USB	universal serial bus
VHDL	very high-speed integrated circuit hardware description language
VHF	very high frequency
VMOD	vector modulator

VNA	vector network analyzer
VOD	video on demand
VSA	vector signal analyzer
VSWR	voltage standing wave ratio
VVA	voltage controlled variable attenuator
VVP	voltage controlled variable phase shifter
WCDMA	wide code division multiple access

SUMMARY

The objective of this research is to implement a hybrid digital/RF envelope predistortion linearization system for high-power amplifiers used in wireless communication systems. It is well known that RF PAs have AM/AM (amplitude modulation) and AM/PM (phase modulation) nonlinear characteristics. Moreover, the distortion components generated by a PA are not constant, but vary as a function of many input conditions such as amplitude, signal bandwidth, self-heating, aging, etc. Memory effects in response to past inputs cause a hysteresis in the nonlinear transfer characteristics of a PA. This hysteresis, in turn, creates uncertainty in predictive linearization techniques. To cope with these nonlinear characteristics, distortion variability, and uncertainty in linearization, an adaptive digital predistortion technique, a hybrid digital/RF envelope predistortion technique, an analog-based RF envelope predistortion technique, and a combinational digital/analog predistortion technique have been developed.

A digital adaptation technique based on the error vector minimization of received PA output waveforms was developed. Also, an adaptive baseband-to-baseband test system for the characterization of RF PAs and for the validation of linearization algorithms was implemented in conjunction with the adaptation technique. To overcome disadvantages such as limited correction bandwidth and the need for a baseband input signal in digital predistortion, an adaptive, wideband RF envelope predistortion system was developed that incorporates a memoryless predistortion algorithm. This system is digitally controlled by a look-up table (LUT). Compared with conventional baseband digital approaches, this

predistortion architecture has a correction bandwidth that is from 20 percent to 33 percent wider at the same clock speeds for third to fifth order IMDs and does not need a digital baseband input signal.

For more accurate predistortion linearization for PAs with memory effects, an RF envelope predistortion system has been developed that uses a combination of analog-based envelope predistortion (APD) working in conjunction with digital LUT-based adaptive envelope predistortion (DPD). The resulting combination considerably decreases the computational complexity of the digital system and significantly improves linearity and efficiency at high power levels.

CHAPTER I

INTRODUCTION

1.1 MOTIVATION

A radio frequency (RF) power amplifier (PA) is a central component in communication systems for the transmission of voice or data signals to mobile units through the air. The enormous expansion of mobile phone subscribers along with multimedia services such as video telephony, video on demand (VOD), digital multimedia broadcasting (DMB), multimedia messaging service (MMS), etc., has driven the increases in capacity of cellular base station transmitters. However, a PA represents a significant fraction of the manufacturing price of a base station transmitter, making it one of the most expensive elements. With this situation in mind, it should be recalled that the PA has AM/AM (amplitude modulation) and AM/PM (phase modulation) nonlinear characteristics. Because of these nonlinear characteristics, input power must be driven at a reduced rate to ensure that transmitted signals are of high quality. Ultimately, this requirement leads to poor efficiency and waste of PA power capacity.

Because of the necessity to cover the increased service demands, next-generation carriers must achieve higher base station capacity in limited space. For this reason, cost and efficiency are of greater concern compared to second-generation (2G) equipment. A

single-carrier power amplifier (SCPA) approach often requires less investment in initial deployment, but the multicarrier approach ultimately supports higher capacity and significantly greater flexibility [1], [2]. Because many third-generation (3G) applications require higher base station capacity in limited space, the multicarrier approach is expected to be the 3G configuration of choice [2]. This has the advantage of simplifying network upgrades, but more importantly, it extends the life of the installed network. Therefore, the service provider can deploy a network that meets the initial capacity demands and has the flexibility to increase the network capacity as demand increases [1], [2]. However, the multicarrier power amplifier (MCPA) system requires a wideband operation, and because of their cross modulation the multicarrier signals place a greater burden on the PA in terms of peak power capability and linearity.

To achieve high bandwidth efficiency, applications such as cdma2000 and WCDMA use complex digital modulation schemes shown in Figure 1.1.

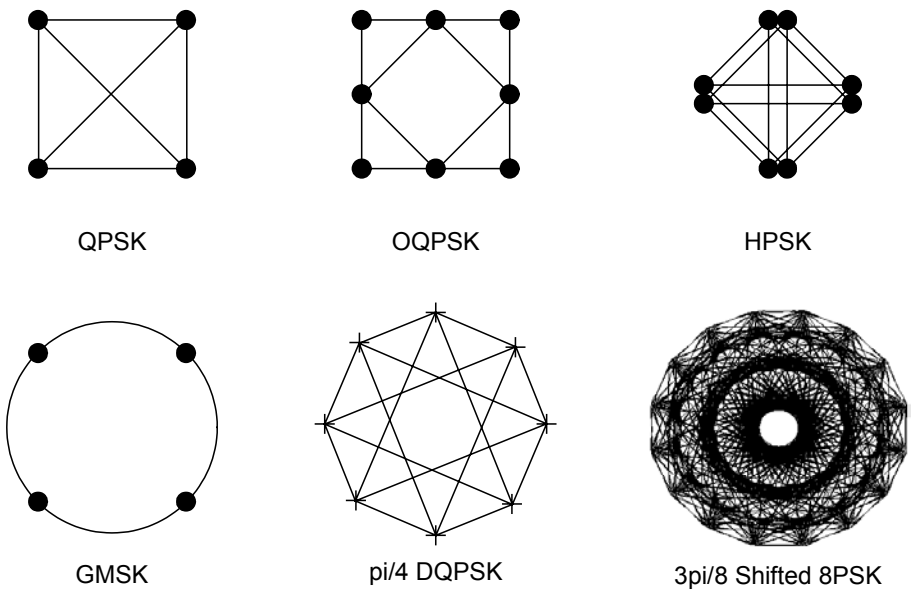


Figure 1.1 Signal trajectory of modern digital modulation techniques.

As shown in Table 1.1, these formats have a high peak-to-average power ratio (PAPR) and inevitably produce high levels of interference because of the significant amplitude and phase distortions inherent in the PA. Moreover, these high peaks can coherently add in a multicarrier system, further increasing the PAPR [2], [3]. Intermodulation distortion (IMD) rapidly degrades when the signal peaks approach amplitude saturation region, thus requiring some backoff of the average power level. In contrast, higher efficiency is obtained as the average power is increased. Therefore, it is desirable to extend the linear range of the PA as high as possible toward the saturation point so as to obtain a reasonable trade-off between linearity and efficiency [3]. To achieve good linearity with reasonable efficiency, some type of linearization technique has to be employed.

Table 1.1 PAPR of wireless communication signal standards.

Modulation			Peak-to-Average Ratio (PAPR)	
			Single Carrier	Multicarrier
2G	cdmaOne (IS-95)	QPSK/OQPSK	10.5	11
	TDMA (IS-54, IS-136)	pi/4 DQPSK	3.5	10.5
	GSM	GMSK	0.5	10.5
3G	cdma2000	QPSK/OQPSK/HPSK	9	9
	WCDMA	QPSK/OQPSK/HPSK	7	7
	EDGE	3pi/8 Shifted 8PSK	3	10

1.2 NONLINEAR RESPONSES OF PAS

Because of the nonlinear characteristics of a PA, the modulation sidebands interact with each other and produce IMDs, as illustrated in Figure 1.2.

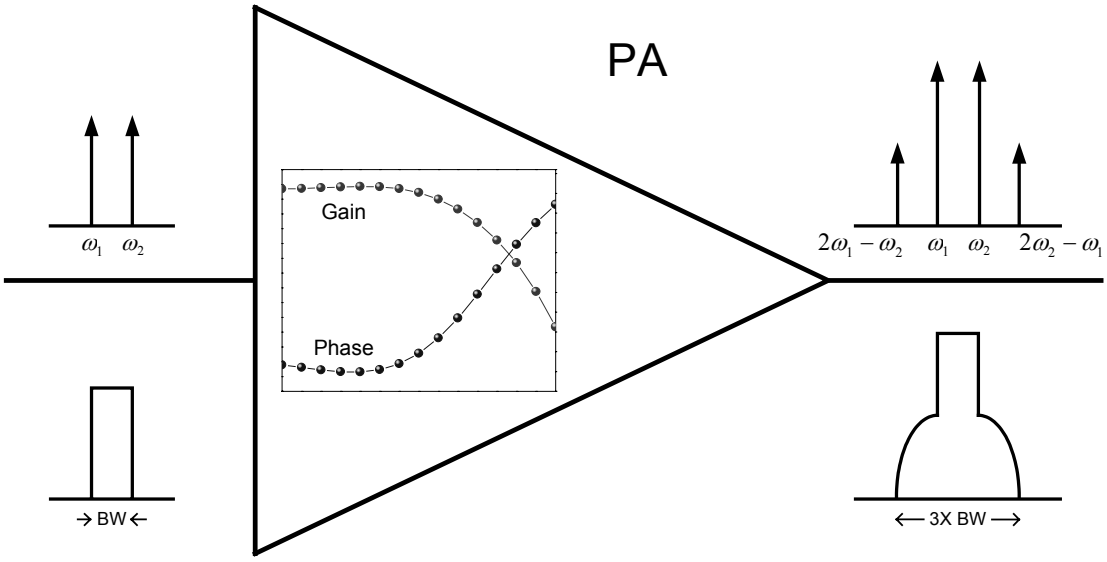


Figure 1.2 PA nonlinear responses for two-tone and CDMA signals.

For simplicity, let's consider a PA that is a memoryless, time-variant system as follows:

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t), \tag{1.1}$$

where a is the complex coefficient. To understand how (1.1) leads to intermodulation, assume that two signals with amplitudes A_1 and A_2 at different frequencies ω_1 and ω_2, respectively, are applied to the nonlinear system as

$$x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t. \tag{1.2}$$

From (1.1) and (1.2), the output signal, which includes fundamental components, second-order products, and third-order products, can be described as

$$\begin{aligned} y(t) = &\left(a_1 A_1 + \frac{3}{4} a_3 {A_1}^3 + \frac{3}{2} a_3 A_1 {A_2}^2\right)\cos\omega_1 t + \left(a_1 A_2 + \frac{3}{4} a_3 {A_2}^3 + \frac{3}{2} a_3 A_2 {A_1}^2\right)\cos\omega_2 t \\ &+ \frac{a_2}{2}({A_1}^2 + {A_2}^2) + a_2 A_1 A_2 \{\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t\} + \frac{a_2}{2}({A_1}^2 \cos 2\omega_1 t + {A_2}^2 \cos 2\omega_2 t) \\ &+ \frac{3a_3 {A_1}^2 A_2}{4}\{\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t\} + \frac{3a_3 A_1 {A_2}^2}{4}\{\cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t\}. \end{aligned} \tag{1.3}$$

As shown in (1.3), the fundamental tones include the nonlinear terms that cause the in-channel distortion as well as the linear gain term. The third-order intermodulation products at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 reveal nonlinearities and are particularly of interest because they are in the vicinity of ω_1 and ω_2 and may not be eliminated by bandpass filtering. These phenomena may be more evident via an experiment. The test setup shown in Figure 1.3 was constructed to measure the interference power produced by a nonlinear PA. Because much of the interference power occurs within the bandwidth of the modulated signal, the undistorted portion must be eliminated to determine accurately the amount of interference power. This is similar to the carrier cancellation loop in a feed-forward linearization. To improve the accuracy of measurement, a single-tone calibration at an intended carrier frequency is first performed using a vector network analyzer (VNA).

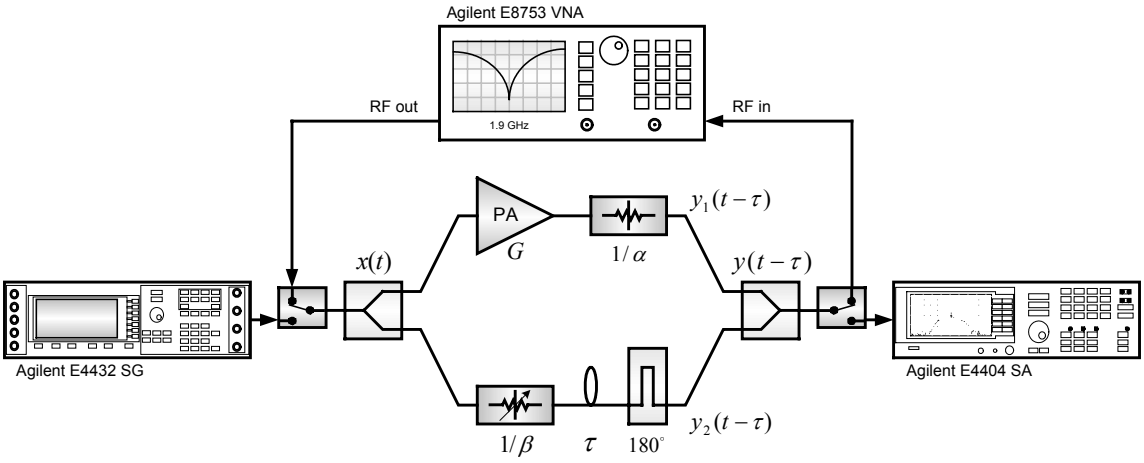


Figure 1.3 Interference signal measurement setup.

On the calibration stage, the VNA generates a single-tone signal $x(t)$ at a carrier frequency ω_c as follows:

$$x(t) = A\cos\omega_c t\,, \tag{1.4}$$

where A is the amplitude of the single-tone signal. Assuming the PA has a group delay of τ, its gain function $G\{\cdot\}$ can be described as

$$G\{|\,x(t)\,|,\tau\} = \sum_{k=1}^{K} a_{2k-1}\,|\,x(t-\tau)\,|^{2(k-1)}\,, \tag{1.5}$$

where $a_{2k\text{-}1}$ is the complex polynomial coefficient. The group delay can be defined and calculated by (1.6) with the transmission coefficient of S-parameters from the VNA, S_{21}.

$$\tau = -\frac{d\theta}{d\omega} \approx -\frac{\theta_{S_{21}}(f+\Delta f) - \theta_{S_{21}}(f)}{2\pi\cdot\Delta f}. \tag{1.6}$$

As illustrated in Figure 1.3, the output $y(t)$, which is delayed by τ, is described as

$$\begin{aligned} & y(t-\tau) = y_1(t-\tau) + y_2(t-\tau) \\ & = \left\{\frac{a_1}{\alpha}x(t-\tau) + \frac{a_3}{\alpha}x(t-\tau)\,|\,x(t-\tau)\,|^2\right\} + \left\{-\frac{1}{\beta}x(t-\tau)\right\} \\ & = \left\{\left(\frac{a_1}{\alpha}-\frac{1}{\beta}\right)\cdot\cos[\omega_c(t-\tau)]\right\} + \left\{\frac{a_3}{\alpha}\cos[\omega_c(t-\tau)]\,|\cos[\omega_c(t-\tau)]\,|^2\right\} \\ & = Carrier + Interference \end{aligned}, \tag{1.7}$$

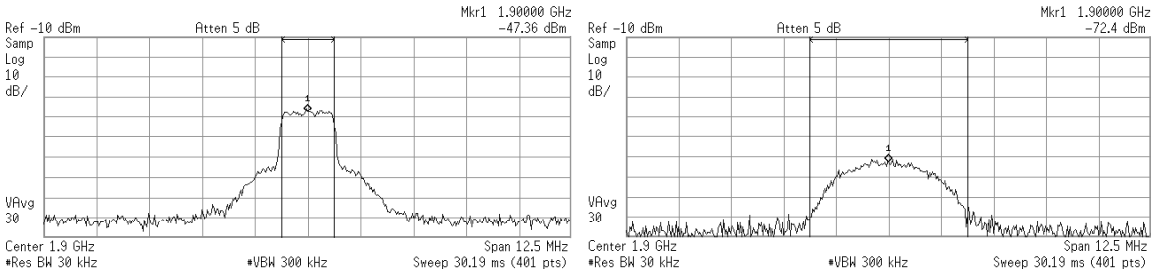
where $1/\alpha$ is the fixed attenuation on the first path, $1/\beta$ is the variable attenuation on the second path, and the interference signal part can be obtained from the carrier signal cancellation by adjusting the variable attenuator as follows:

$$\beta = \frac{\alpha}{a_1}, \tag{1.8}$$

where α should be larger than the linear gain term a_1 to avoid the use of an active component on the second path.

Figure 1.4 shows the spectrum results before and after carrier cancellation for a cdmaOne signal. The interference power forming side lobes around the carrier signal

results in the degradation of signals in adjacent channels, while the interference within the signal channel increases the bit-error rate (BER) on the carrier signal. Also, because the closely adjacent characteristic of the intermodulation products, it is difficult to remove them by filtering. Therefore, a linearization technique must be used to keep within the regulations governing wireless communications and preserve signal quality at the same time.



(a) (b)

Figure 1.4 Spectra for a cdmaOne forward link nine-channel signal with a signal bandwidth of 1.2288 MHz. (a) Before the in-channel signal cancellation. (b) After the in-channel signal cancellation.

1.3 PA LINEARIZATION

A wide range of linearization techniques has been proposed for modern communication system applications. These techniques can be roughly classified into three groups: (1) feedback, (2) feedforward, and (3) predistortion. Among these techniques, predistortion may be the most viable solution because of reasonable trade-offs between linearization performance and cost over a wide frequency bandwidth.

1.3.1 Feedback Technique

The feedback (FB) technique is commonly known as the simplest and most obvious method of reducing amplifier distortion. Harold S. Black invented a negative FB technique as a way as to solve the distortion problem of the positive FB [4], [5].

The simplest negative FB technique applied to RF amplifiers is RF FB, as shown in Figure 1.5. It includes passive FB [4]-[6] and active FB [7], [8] techniques. Since RF amplifiers display much larger phase shifts and electrical length at gigahertz frequencies, the electrical delays around the FB loop restrict the bandwidth of signals that can be linearized. This restriction ultimately leads to instability. Therefore, the RF FB has bandwidth limitations in high-frequency applications and is commonly used at low frequencies.

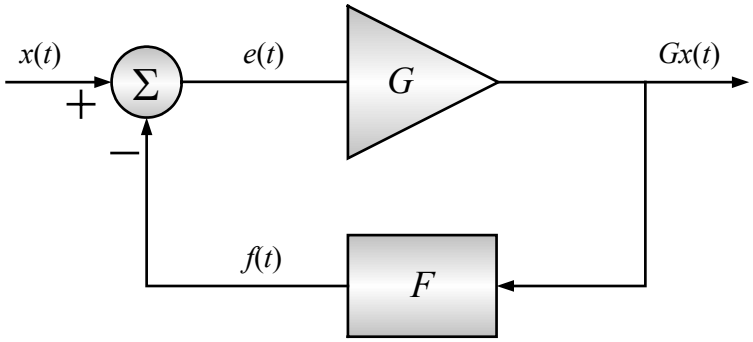


Figure 1.5 RF feedback amplifier.

To eliminate the drawback of group delay problems in the RF FB techniques, envelope feedback (EFB) techniques using envelope amplitude and phase variations offer some possibilities for bypassing fundamental phase delay problems. Figure 1.6 shows the EFB amplifier. Arthanayake and Wood proposed an EFB [9]. By using this technique, they

could use multistage FB amplifiers to get high power gains efficiently. Recently, Cardinal *et al*. proposed an adaptive double EFB technique using a dynamic gate bias in conjunction with a voltage-controlled phase shifter [10].

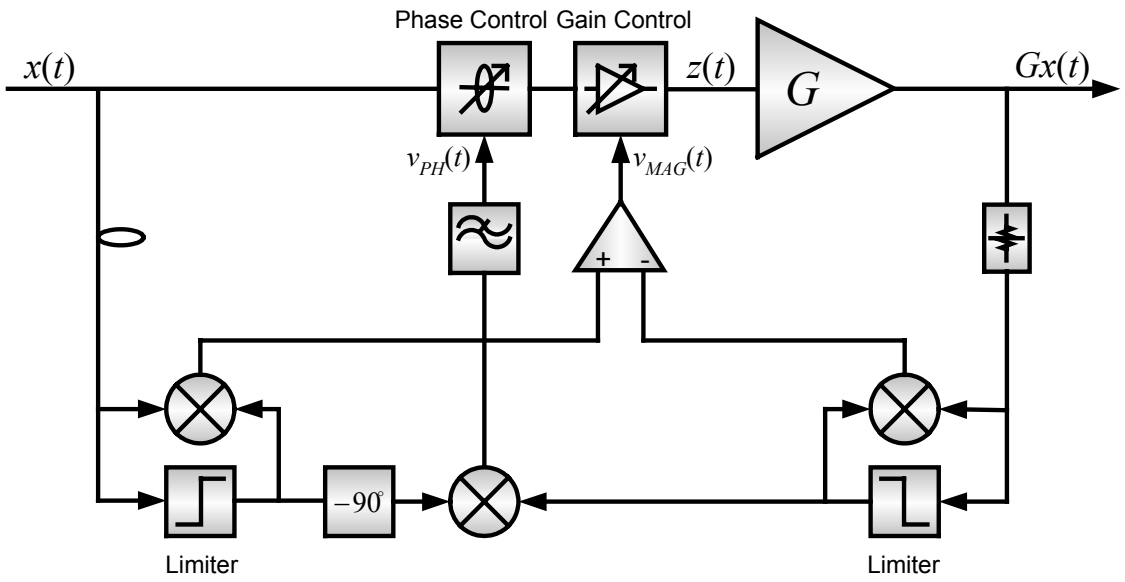


Figure 1.6 Envelope feedback amplifier.

Cartesian feedback (CFB) techniques separate the signal into in-phase and quadrature-phase components. This eliminates the need for phase shifters and still allows the correction of gain and phase by adjusting the amplitudes of two orthogonal components. In this architecture, detection must be done synchronously (quadrature detection) [11]. An advantage of the CFB is that the bandwidths of the in-phase and quadrature components are approximately equal, unlike polar form EFB systems in which the bandwidth of the phase component is much greater than that of the amplitude component. Although these alternative FB techniques mitigate the delay problem, they also suffer from problems such as misalignment.

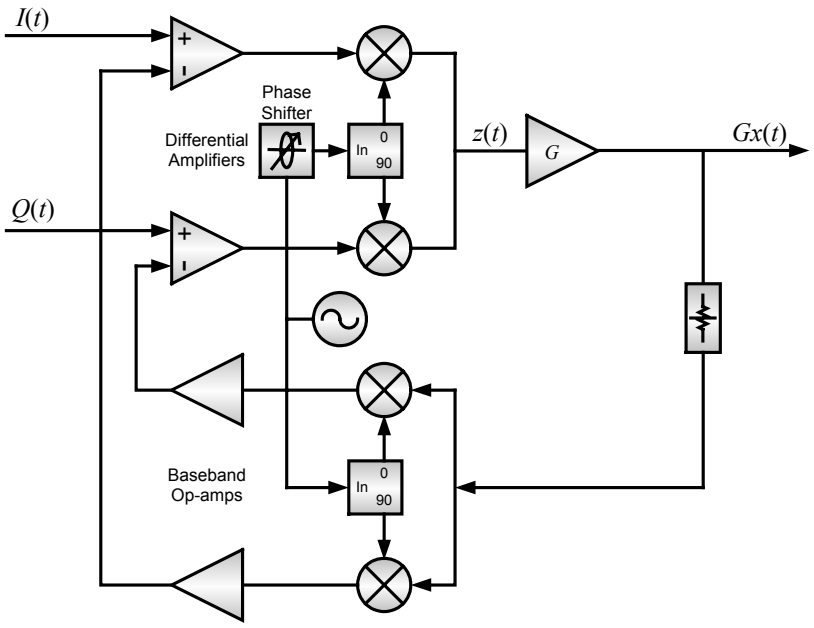


Figure 1.7 Cartesian feedback amplifier.

The principal limitation of FB techniques is an inability to handle wideband signals. In practice, it is difficult to make an FB system respond to signal-envelope changes much greater than several MHz because of the delay of the amplifier and associated signal processing components. RF/Microwave amplifiers for a base station may consist of multiple PA stages and have delays of 10-20 *ns*.

1.3.2 Feedforward Technique

The feedforward (FF) technique is the most popular PA linearization technique for a base station application because of its outstanding performance in IMD correction [3]. Harold S. Black, who is generally recognized as the inventor of the FB technique, also invented the FF technique in 1928 [12]. His basic idea for the FF technique was to build two identical amplifiers and use one amplifier to subtract the distortion from the other, although the

power capacity of the error power amplifier (EPA) used in modern FF systems is often from 10 percent to 25 percent of the saturation power of the main amplifier. Figure 1.8 describes the FF system architecture. The output of the main amplifier feeds a perfectly linear attenuator. The attenuated output is then subtracted from the input to yield a signal that is a perfectly scaled version of the distortion. This pure distortion signal feeds the EPA. The distortion signal from the EPA is subtracted from the distorted signal of the main amplifier to yield a final output that has greatly reduced distortion. Since its correction is not based on a past event, it is independent of the amplifier delays, making the system unconditionally stable. Moreover, it does not reduce amplifier gain. The modern application in the RF use of FF began with the work of Seidel *et al.* at Bell Laboratories [13].

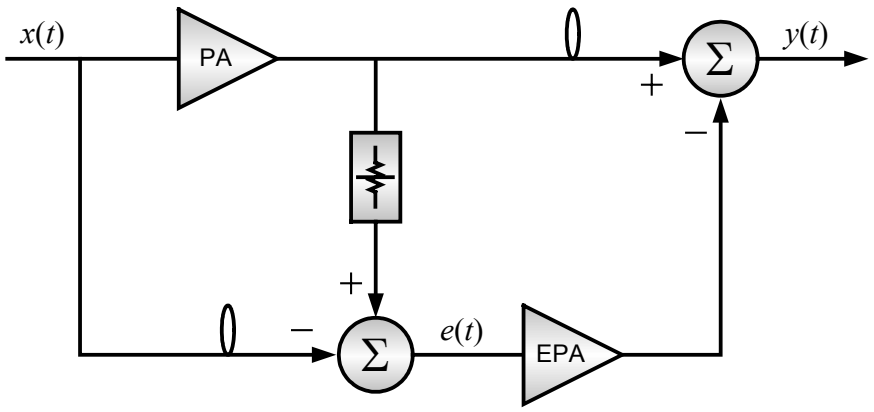


Figure 1.8 Feedforward amplifier.

Changes of device characteristics with time and temperature are not corrected because of its open-loop nature. Therefore, an adaptive control method is essential in FF linearization [14]. Various adaptive control approaches have been proposed. A fixed pilot tone method

[15], pilot tone hopping method [16], gradient method [17], a combination of the pilot tone hopping and the gradient [18], and an intentional signal perturbation method have all been reported [19]. Figure 1.9 shows an adaptive FF amplifier using a pilot signal.

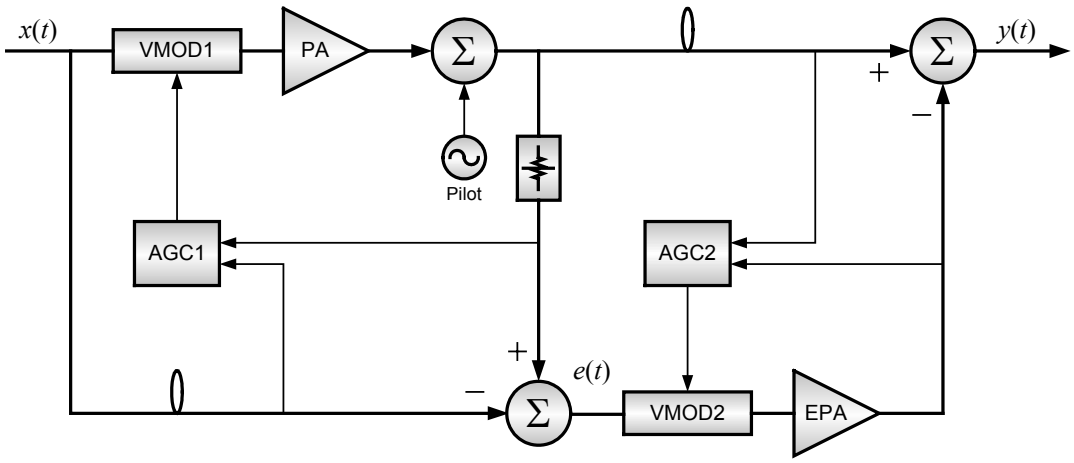


Figure 1.9 Adaptive feedforward amplifier using a pilot signal.

Nevertheless, a high degree of matching between the cancellation elements in both amplitude (< 0.25 dB for over 30 dB correction) and phase (< 2° for over 30 dB correction) must be maintained over the correction bandwidth of interest [2]. Although the adaptive control methods mentioned above are employed, it is not easy to simultaneously maintain both amplitude and phase over the correction bandwidth within such a high degree. Moreover, an error amplifier, a delay line, and combiners are required at the output of a main PA to compensate for the IMDs and cause a large amount of insertion loss and circuit complexity, ultimately leading to poor efficiency.

1.3.3 Predistortion Technique

Predistortion (PD) simply involves the creation of a distortion characteristic that is

precisely opposite to the distortion characteristic of the RF PA, cascading the two to ensure that the resulting system has little or no input-output distortion. Various predistortion techniques have been proposed as alternative solutions to FF linearization. Since linearization is performed at the input of the PA, loss of efficiency is negligible. Predistortion techniques can be classified into analog PD, digital PD, and hybrid PD.

Analog PD linearizers, shown in Figure 1.10, are small and inexpensive and work at RF frequencies.

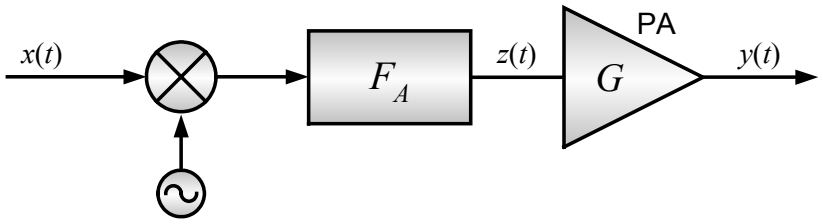


Figure 1.10 Analog predistortion.

However, because analog predistorters typically fall short of the accuracy required for correcting all of the terms involved, they typically have been used to focus on the third –order intermodulation components for low PAPR signals [20]. To compensate for higher-order IMDs in multicarrier systems, more complex circuits may be required [21]. Moreover, automatic control circuitry is often needed to ensure tracking over all corners of the operational specification [22].

The digital baseband PD methods shown in Figure 1.11 have been popular in recent years because, compared with analog systems, they are more accurate [23]-[25].

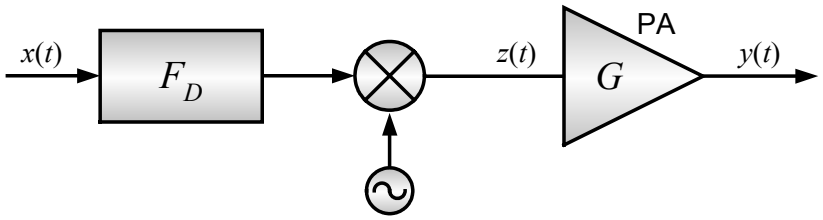


Figure 1.11 Digital predistortion.

The digital PD technique is very popular these days because of its accuracy in signal processing. Processing speeds for digital signal processors are now sufficient to treat signals with bandwidths in excess of 20 MHz. These techniques, however, have disadvantages in terms of system architecture because the digital PD technique must depend on a digital baseband input, and the computational speed of the digital circuits limits the operational bandwidth. Moreover, since power consumption of a DSP processor is directly related to operating frequency, higher computational speed leads to higher power consumption [26].

As a compromise between analog RF PD and digital baseband PD, the hybrid RF envelope predistortion architecture shown in Figure 1.12 has been studied recently [27]-[30]. Compared with analog approaches, this predistortion architecture, which uses an adaptive DSP technique, achieves more accurate linearization.

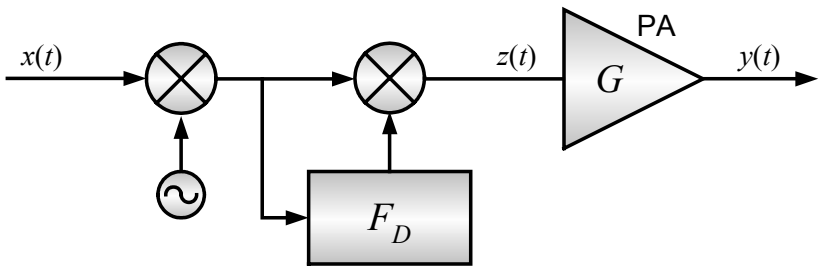


Figure 1.12 Hybrid digital/RF predistortion.

In addition, this architecture has advantages over conventional baseband digital approaches in that instantaneous correction occurs through the use of RF circuits without being limited by DSP speed, and a 20-33 percent wider correction bandwidth is achievable for third to fifth order distortions at the same clock speeds. Since it is nonparametric and does not rely on any knowledge of the signal structure, linearization can be performed without the need for a digital baseband input signal. Therefore, the hybrid PD techniques are also suitable for repeater systems. These are devices that further help extend signal coverage between a base station and wireless handsets by relaying signals to areas where the base station signal is not available. By using a repeater, signals can be preserved even in such shadowed areas as underground parking lots, subways, building interiors, etc. To the best of the authors knowledge, the first hybrid predistortion system architecture, which employed an adaptive polar analog work-function predistortion, was demonstrated by Rey in [27]. A subsequent predistortion architecture used an I/Q vector modulator to predistort an RF input signal [28]. Because this architecture extracts the reference signal after the I/Q modulator, the nonlinear behavior of the modulator cannot be corrected. Kusunoki *et al*. implemented a similar architecture for cellular phones based on polar envelope predistortion [29]. Gentzler *et al*. also patented a comparable architecture that uses analog circuits to extract PA characteristics [30].

1.4 PA MEMORY EFFECTS

1.4.1 Characteristics of Memory Effects

The distortion components generated by a PA are not constant, but vary as a function of

many input conditions such as amplitude, signal bandwidth, self-heating, aging, etc. The phenomena in which the output response is dependent on the past inputs as well as on the input at the current time instant are called *memory effects* [31]-[34]. Memory effects cause a hysteresis in the nonlinear transfer characteristics of a PA, which creates an uncertainty in the model for distortion prediction. The memory effects can be classified into three types: (1) RF frequency response, (2) envelope frequency response, and (3) electro-thermal feedback response [31]-[34]. RF frequency response is a short-time constant memory effect caused by the instantaneous frequency response of the PA over RF frequencies. Envelope frequency response comes from the low-frequency response of bias circuits interacting with even-order products at baseband frequencies. Also, electro-thermal feedback response causes a shift in gain or phase as a result of self-heating and hence also contributes to the envelope frequency response. While RF frequency response and bias-related effects may be reduced by careful design [35], thermal effects are not so easily removed. The thermal effects may be reduced by careful die design. However, their treatment at the device level may only be achieved by reducing the thermal impedance of the substrate that requires unnecessarily large device geometries or the use of exotic materials. Figure 1.13 illustrates the most sensitive parts leading to memory effects in widely used biasing circuits for bipolar and FET amplifiers. According to [31], [33], short-time constant ($\leq 1\mu s$) memory effects are caused by the parasitic of the RF choke coil and the resonance frequency of the bypassing capacitor in response to the input signal envelope. On the other hand, long-time constant ($> 1\mu s$) memory effects are typically due to the thermal time constants of the devices and some of the components in the biasing circuit.

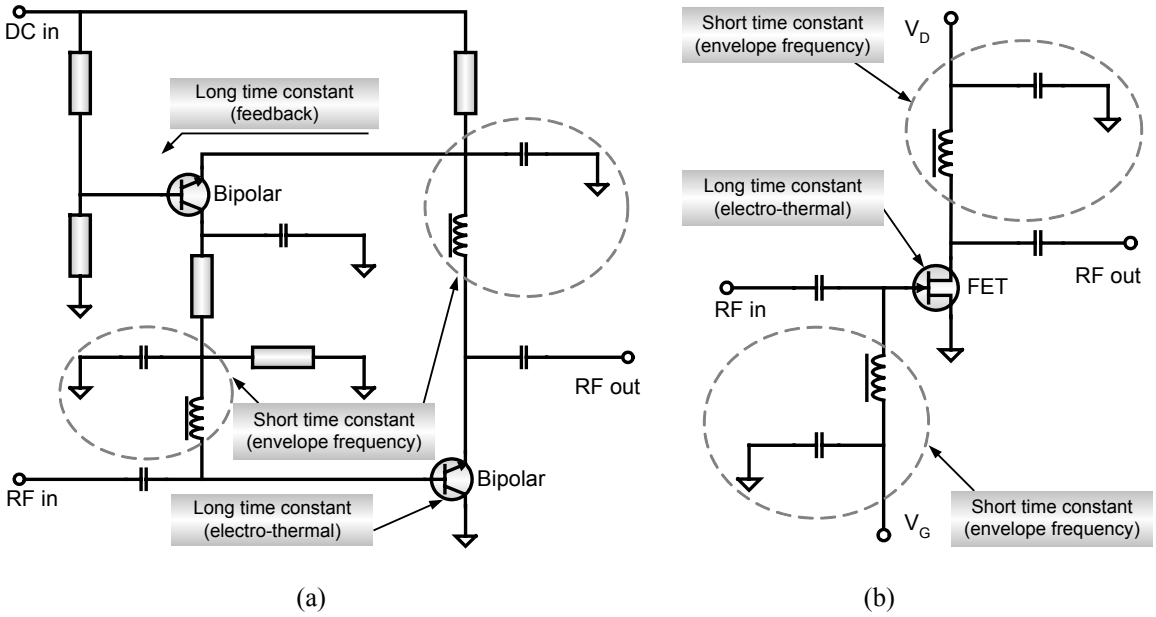


Figure 1.13 Typical location of memory effects. Biasing netwoks for (a) bipolar and (b) FET amplifier [31].

The primary indication of PA memory effects is the variation in two-tone IMD versus tone spacing [31]. In addition, this baseband frequency response may vary as a function of signal level. Figure 1.14 shows the test setup using two-tone signals to measure IMD variations over tone spacing and power.

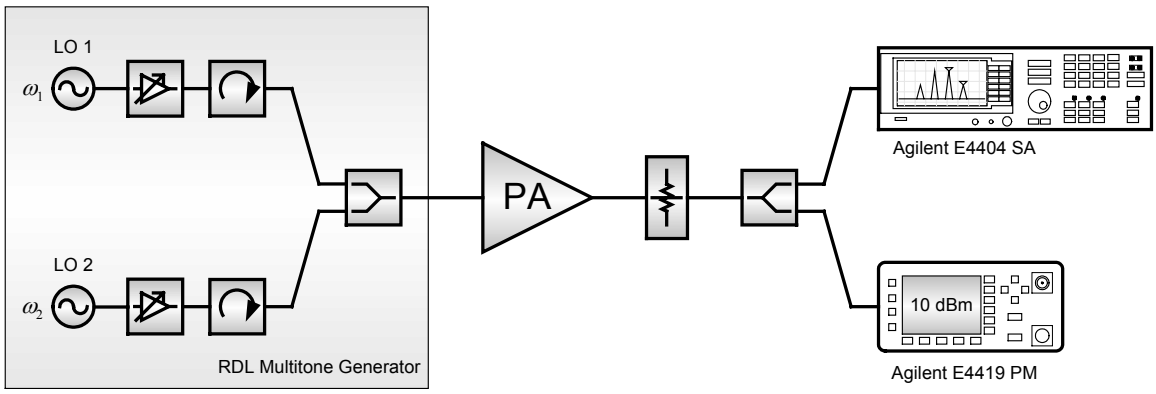
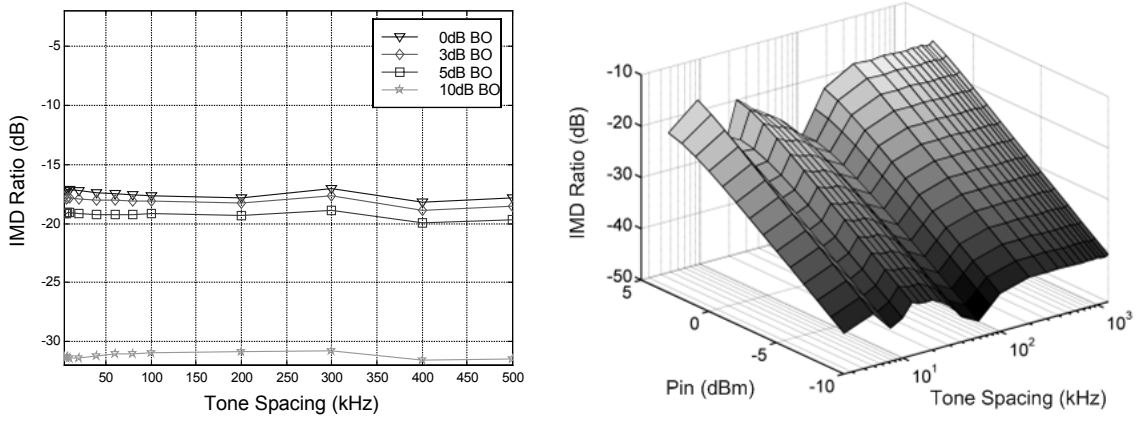


Figure 1.14 Two-tone test setup.

Two single-tone signals are generated by a multitone generator with a series of tone-spacings $|\omega_1-\omega_2|$ and power levels. The output signals passed through a PA are then attenuated to within the allowed input power range of measurement equipment such as a spectrum analyzer and a power meter.

Figure 1.15 shows the results measured from the test setup. Figure 1.15a shows the two-tone IMD of the Sirenza Microdevices 0.5W PA. The variation of IMD versus tone spacing is seen to be small (less than 2 dB) from 1 kHz to 500 kHz. In contrast, as shown in Figure 1.15b, the IMD response for the Ericsson 45W class-AB PA as a function of tone spacing and input power is quite variable. It is apparent from the data presented in Figure 1.15 that feedback effects resulting from multiple physical sources with different time constants manifest themselves in signals with baseband frequencies below 500 kHz. Therefore, the memory effects of a PA may cause uncertainty of predistortion linearization and decrease the IMD suppression performance of predistortion techniques that do not consider memory effects.



(a) (b)

Figure 1.15 Measured two-tone IMD as a function of tone spacing and power. (a) 0.5W PA. (b) 45W PA.

1.4.2 Identification Techniques

As mentioned in the previous section, predictive systems like predistortion are vulnerable to any changes in the behavior of the PA, and memory effects may cause severe degradation in linearization performance. In practice, it is quite difficult to predict memory effects under varying signal conditions. However, because the behavior of the spectral components is certainly deterministic, compensation for memory effects may be achieved, making predistortion linearization techniques more applicable to nonlinear high-power amplifiers.

High predistortion performance ultimately depends on how accurately nonlinear characteristics can be obtained. The approaches to nonlinear modeling based on the Taylor series and the orthogonal series and the direct transform methods of nonlinear system analysis are simple but suitable only for memoryless nonlinearities. The development of more complex models to deal with nonlinear systems with memory dates back to the late 19th century.

Volterra published a functional series expansion in 1887 that is well known as the *Volterra series* [36]. The Volterra series $y_v(t)$, which is defined in (1.9), is a general nonlinear model with memory and has been used to describe PAs with mild nonlinearity [37].

$$\begin{aligned} y_v(t) = h_0 &+ \int_{-\infty}^{\infty} h_1(\tau_1)x(t-\tau_1)d\tau_1 + \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h_2(\tau_1,\tau_2)x(t-\tau_1)x(t-\tau_2)d\tau_1 d\tau_2 \\ &+ \cdots + \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\cdots\int_{-\infty}^{\infty} h_n(\tau_1,\tau_2,\cdots,\tau_n)x(t-\tau_1)x(t-\tau_2)\cdots x(t-\tau_n)d\tau_1 d\tau_2\cdots d\tau_n + \cdots \end{aligned}, \quad (1.9)$$

where h_0 is the DC term, the multidimensional function $h_n(\tau_1,\tau_2,\cdots,\tau_n)$ is called the

n*th-order kernel* or the n*th-order nonlinear impulse response*, and the excitation function $x(t-\tau_n)$ is any finite small-signal voltage or current waveform. In 1942, Wiener was the first to apply the Volterra theory to analyze a nonlinear device [38], [39]. Methods of measuring Volterra kernels were published by Schetzen in 1965 [40]. A serious drawback of the Volterra model is the large number of coefficients that must be extracted, and the measurement is difficult because of the cross-coupling among the Volterra kernels. Wiener developed an orthogonal representation of nonlinear systems with memory and subsequent measurement methods for Wiener kernels [41]. The formulation of the Wiener model of nonlinear systems was a major breakthrough for kernel measurements. The orthogonality of the Wiener functionals for a white Gaussian input allowed the Wiener kernels to be easily measured using cross-correlation techniques. In 1961, the work by Lee and Schetzen led to a Wiener kernel identification technique known as the Lee-Schetzen method [42]. Schetzen later generalized the Wiener theory to nonwhite Gaussian inputs and extended the cross-correlation measurement method for this class of inputs [43]. He also developed the theory of p*th order Volterra inverses* [44]. The Volterra and Wiener representations are both nonlinear moving average models that use functionals and kernels for modeling a wide class of nonlinear systems with memory. Under suitable continuity conditions, the Volterra and Wiener models with truncated nonlinearity order and memory can be used to represent nonlinearities, to an arbitrary accuracy, over a given input amplitude range. The identification of Hammerstein models, which are the reverse version of the Wiener models in the structure sequence, has been studied since the late 1960s when Narendra and Gallman proposed an identification procedure using an iterative method [45].

The Wiener, Hammerstein, and Wiener-Hammerstein models, which are shown in

Figure 1.16, are widely adopted in nonlinear PA modeling based on block-oriented approaches. Various identification algorithms have been proposed for these models in which the parameters of the nonlinear element and linear dynamics are obtained simultaneously or iteratively. The nonlinear element describes the frequency-independent nonlinear characteristics of a PA, while the linear element represents the frequency-dependent characteristics of the broadband signals.

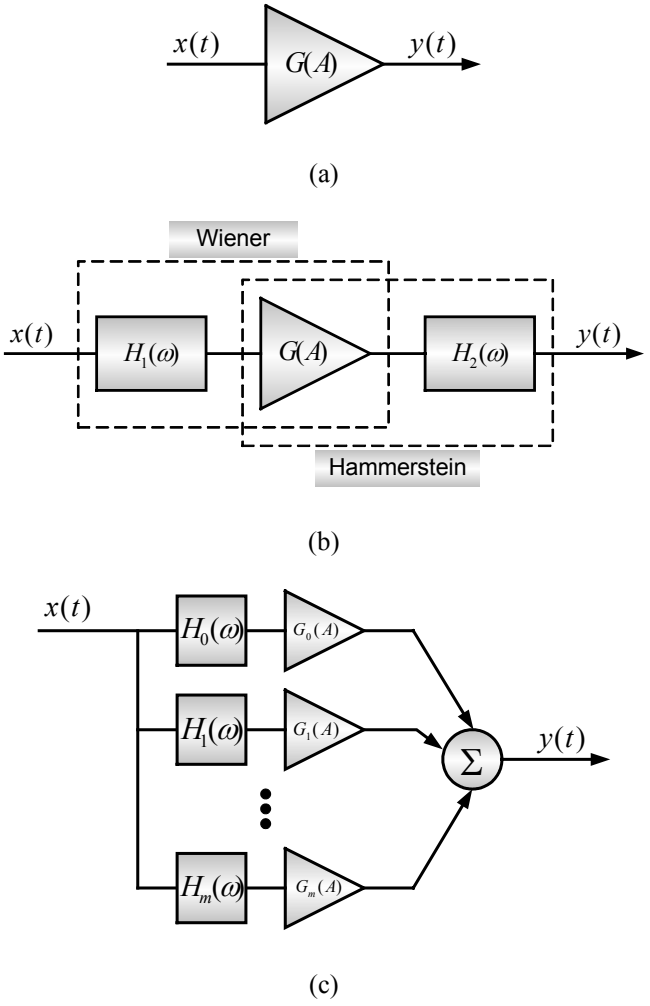


Figure 1.16 Block-oriented PA models. (a) One-box nonlinear model. (b) Three-box Wiener-Hammerstein model. (c) Parallel Wiener model.

In recent years, special cases derived from the Volterra and Wiener models have been proposed, based on the block models, to capture in the PA the memory nonlinear effects associated with wideband signals. Clark *et al*. proposed a Wiener-type PA model [46]. As an expanded Wiener model for PAs, Ku *et al*. proposed a parallel Wiener PA model [47]. Another model, which is described in (1.10), is the memory polynomial model proposed by Kim *et al*. [48].

$$y_{mp}[n] = \sum_{q=0}^{Q} x[n-q] \sum_{k=1}^{K} a_{q,k} \left| x[n-q] \right|^{k-1}, \tag{1.10}$$

where $a_{q,k}$ are complex coefficients, Q is the length of the memory, and K is the order of nonlinearity. Similar to the Volterra model, an exact inverse of the memory polynomial is difficult to obtain, but another memory polynomial can be constructed as an approximate inverse by truncating various terms in the Volterra series. On the other hand, using the standard unit sample delay to model memory effects present at low envelope frequencies may require a very large number of delay taps. An adaptive delay method can model the low-frequency envelope response with very few elements because the delay taps can spread out to track the low-frequency responses of the PA memory effects. Thus, only delay taps with information about the system are required. Etter *et al*. proposed the delay adaptation method to model a filter with sparse delay taps [49]. Ku *et al*. employed this method to model a PA with memory effects and achieved an accurate behavioral PA model [50]. Equation (1.11) shows the memory polynomial model with the sparse delay taps.

$$y_{sd}[n] = \sum_{q=0}^{Q} x\left[n-\tau_q\right] \sum_{k=1}^{K} a_{2k-1,q} \left| x\left[n-\tau_q\right] \right|^{2(k-1)}, \tag{1.11}$$

where τ_q is the delay value on the q^{th} tap.

1.4.3 Compensation Techniques

In recent years, there has been intensive research on memory effect compensation using DSP techniques. Compensation for memory effects involves the use of memory within the predistortion model. Predistorters using a truncated Volterra series have usually been implemented by the *p*th-order inverse technique [51]. However, the implementation of a *p*th-order inverse system can be very complicated and must be based on a known Volterra series model of the nonlinear PA. Eun *et al*. proposed a Volterra predistorter using an indirect learning architecture to avoid the prior modeling of PA response [52]. By using a predistorter based on the memory polynomial model, Kim *et al*. reduced computational complexity considerably [48]. Ding *et al*. proposed a memory polynomial predistorter in conjunction with the indirect learning architecture [53]. This combination made it easier to accurately obtain the predistortion function and achieved good predistortion performance for different PA models. However, its implementation is complicated by the additional data required to identify the coefficients associated with the memory effects. Moreover, as the techniques are applied to high-power base station amplifiers operating near compression, increasingly longer delays and higher order polynomials are required to compensate for thermal feedback [33]. Such long delays greatly increase the computational complexity of the predistortion technique, requiring expensive and power hungry high-speed DSP.

Recently, a new digital/analog envelope predistortion linearization system was developed for PAs with low-frequency memory effects [54]. A digital LUT-based adaptive predistortion system was used to compensate for instantaneous distortion resulting from the memoryless portion of the PA nonlinear transfer characteristic. An analog envelope

predistortion system, implemented with commercially available components, was inserted to compensate for long-time constant envelope memory effects. The resulting combination considerably decreases the computational complexity load of the digital system and significantly improves linearity and efficiency at high power levels.

1.5 DISSERTATION OUTLINE

The remainder of this dissertation consists of five main chapters followed by a chapter on conclusions drawn from this research. Much of the work is on RF envelope predistortion linearization techniques for PAs and implementation methods. Other sections of the work would be relevant to the compensation for memory effects of HPAs in base station transmitters. A comprehensive outline of the work contained in this dissertation is given below on a chapter-by-chapter basis.

Chapter 2: Adaptive Digital Predistortion

The main purpose of this chapter is to develop an automated digital predistortion test system for developing an adaptive predistortion linearization algorithm and validating its feasibility in conjunction with commercially available RF PAs. The AM/AM and AM/PM distortion introduced by a PA act adversely on signal quality metrics such as adjacent channel power ratio (ACPR), error vector magnitude (EVM), and bit-error ratio (BER) in the transmission of complex modulated signals. A digital adaptation technique based on the error vector minimization of PA output waveforms is used to achieve both precise and stable distortion compensation performance.

Chapter 3: Hybrid Digital/RF Envelope Predistortion I: Design and Simulation

This chapter seeks to define and optimize a wideband multicarrier PA system using a hybrid digital/RF envelope predistortion technique. System-level design and simulation approaches, which are described in this chapter, are in demand for designing mixed-signal systems and for tight time-to-market requirements. The simulation of RF and digital signals has been problematic because RF components are generally simulated in the frequency domain at the circuit level, whereas the digital subsystem is simulated behaviorally in the time domain. Moreover, increasing system complexity, reduced size, and faster production cycles drive the need for full system-level simulation and optimization. The behavioral technique used in the system simulation allows for trade-offs to be made between the digital subsystem and the RF component design so as to optimize system performance.

Chapter 4: Hybrid Digital/RF Envelope Predistortion II: Prototype Implementation and Experiments

The purpose of this chapter is to implement and verify the hybrid digital/RF envelope predistortion linearization system, based on the system-level simulation results. The advantages of this predistortion architecture over conventional baseband digital approaches are that a 20-33% wider correction bandwidth is achievable at the same clock speeds, and it can perform linearization without the need for a digital baseband input signal. A memoryless look-up table (LUT) is employed for stable and precise adaptation. It is indexed by a digitized envelope power signal, and instantaneously adjusts the input signal amplitude and phase via an RF vector modulator to compensate for the AM-AM and AM-PM distortion. The operation of this system is validated using various PAs to assure

proper operation of the FPGA LUT and adaptation algorithm.

Chapter 5: Analog Envelope Predistortion

The purpose of this chapter is to develop a new RF envelope predistortion linearization architecture that uses low-power analog components to correct IMD in RF PAs. A complex gain detector based on log amps is used to estimate the instantaneous complex gain by comparing the input and output of the PA. The outputs of the complex gain detector are fed back to the voltage-controlled variable attenuator (VVA) and phase shifter (VVP) to correct any errors in the gain resulting from AM-AM or AM-PM distortion. As opposed to traditional envelope feedback approaches, this architecture achieves greater bandwidth by only feeding the distortion components back and minimizing the number of devices for envelope signal processing. Moreover, the distortion components are not added to the input signal as feedback, but they are used to predistort the input signal in a multiplicative manner. This architecture also allows correction of envelope memory effects that may occur in the PA.

Chapter 6: Envelope Predistortion for PAs with Memory Effects

The purpose of this chapter is to develop an RF envelope predistortion linearization system that uses a combination of an analog envelope predistortion (APD) working in conjunction with a digital LUT-based adaptive envelope predistortion (DPD). The APD system is used as an inner loop to correct for slowly varying changes in gain, effectively compensating for long-time constant memory effects. The DPD forms the outer loop that corrects the distortion over a wide bandwidth. The APD/DPD combination showed a significant ACPR improvement over the DPD alone.

Chapter 7: Conclusions

Important summaries, conclusions, and suggestions for future work are given in this chapter.

1.6 SUMMARY OF ORIGINAL CONTRIBUTIONS

This dissertation makes several original contributions to system architecture design with regard to PA predistortion linearization. In addition, further contributions are made specially to the mixed-signal simulation and system implementation methods for the hybrid digital/RF system. A detailed list of original contributions is given below. In cases in which the work has already been published, details of the associated publications are given.

Chapter 2:

The original contributions of this chapter are as follows:

- An automated baseband-to-baseband test system was developed to easily test a DSP-based adaptive predistortion linearization algorithm and to validate its feasibility in conjunction with commercially available RF PAs.
- A digital adaptation technique, which uses the error vector minimization of PA output waveforms, was developed so that there is no need to hold input baseband signal data.

This work was published in *Proc. of the 57th Automatic RF Techniques Group Conference*, 2001 [55].

Chapter 3:

The original contributions of this chapter are as follows:

- A mixed-signal system simulation method was developed, and a hybrid digital/RF envelope predistortion system architecture was defined.

Some of this work was published in *Proc. of the IEEE Behavioral Modeling and Systems Workshop*, 2002 [56].

Chapter 4:

The original contributions of this chapter are as follows:

- An open-loop predistortion system using an FPGA LUT for predistortion and a VNA for PA characterization was developed, validating the RF envelope predistortion system.

This work was published in *Proc. of the IEEE Radio and Wireless Conference*, 2003 [57].

- A closed-loop predistortion system incorporating the open-loop predistortion system was developed, validating the adaptive hybrid predistortion system architecture.

Some of this work was published in *the IEEE International Microwave Symposium Digest*, 2004 [58], and in *the IEEE Transaction on Microwave Theory and Techniques*, vol. 53, no. 1, 2005 [59].

Chapter 5:

The original contributions of this chapter are as follows:

- A new envelope predistortion linearization architecture was developed, which

utilizes a direct distortion inverse technique and low-power analog components to correct AM-AM and AM-PM distortion in RF PAs.

This work was published in *Proc. of the IEEE Radio and Wireless Conference*, 2004 [60].

Chapter 6:

The original contributions of this chapter are as follows:

- A predistortion linearization system was developed for PAs with low-frequency envelope memory effects. This system is based on the combination of the analog envelope predistortion and digitally adaptive envelope predistortion.

This work is to appear in *the IEEE International Microwave Symposium Digest*, 2005 [54].

CHAPTER II

ADAPTIVE DIGITAL PREDISTORTION

Adaptive digital predistortion, based on the difference between the desired modulation signal and the output of a PA, provides an effective method for PA linearization that continuously adjusts for component drift and power variations. Digital predistortion possesses two advantages. First, the signal processing is applied before the PA, thus insertion loss does not significantly affect PA efficiency. Second, significant IMD reductions can be achieved through accurate mathematical calculations. Digital predistortion, however, has three primary disadvantages: its relative complexity, the need for a baseband input signals, and bandwidth limitations that are linked to the accuracy and computational speed of the specific DSP processor used in the system.

This chapter presents a baseband-to-baseband test system to characterize digital predistortion algorithms. The system operates based on a digital adaptation method that uses the error vector minimization of PA output waveforms. This system permits the testing of algorithms for digital predistortion in automated fashion and simulates the performance of a real-time DSP processor operating in conjunction with actual RF PA circuits. Full characterization capability to 6 GHz and up to 3.7 MHz of baseband bandwidth at 6X oversampling rate is available. The utility of the system is demonstrated with a GaAsFET

PA linearized for CDMA use at 1.9 GHz. LUTs are used to adaptively compensate for amplitude and phase distortion extracted iteratively from oversampled baseband data.

2.1 INTRODUCTION

Digital baseband predistortion methods using DSP have been popular in recent years because of their inherent accuracy [23]-[25]. DSP algorithms are used to predistort baseband data and minimize PA distortion. Using such algorithms, a number of iterations are presumably performed for adaptation. The adaptation is essentially based on learning the gain and phase characteristics of the amplifier at various instantaneous power levels of known training sequences or random data sequences [61].

There are several sources that, in the transmission portion of a communication link, cause signal distortion. These sources include nonlinear amplitude frequency response, nonlinear group delay, intermodulation distortion, noise, etc. These have an impact on signal transmission quality. Error vector magnitude (EVM) is a simple, quantitative figure of merit for a digitally modulated signal and an effective method for both characterizing signal distortion and calculating overall performance of communication systems [62], [63]. Using measurements of instantaneous error vectors, a predistortion algorithm may calculate the instantaneous distortion from the PA and from other errors on the transmission path. Baseband systems can easily be made adaptive if the output signal is demodulated and compared with the reference value. A contemporary vector signal analyzer (VSA) is able to measure errors by generating an ideal reference signal internally and comparing it with the measured signal [64]. Using this type of mechanism, distortion measurement can be performed without a complete communication system being involved.

This chapter presents a fully automated RF/DSP test system to create arbitrary baseband signal envelopes, generate modulated RF signals, and analyze the nonlinear effects of a PA on digitally modulated signals. Using this system, algorithms for baseband predistortion may be tested in an automated fashion. Also, this system may be used to simulate the performance of a real-time DSP processor operating in conjunction with commercially available RF PAs.

2.2 ERROR VECTOR MAGNITUDE

EVM, as defined in (2.1), is a figure of merit for the characterization of transmission quality and an effective method for calculating the overall performance of communication systems.

$$EVM_{rms} = \sqrt{\frac{\sum_{n} |\chi_n - \gamma_n|^2}{\sum_{n} |\gamma_n|^2}}, \tag{2.1}$$

where χ_n is the measured waveform, γ_n is the reference waveform, and n is the sample index. The EVM provides insight into the quality of signals. It may be used as a measure of the difference between the reference and measured waveform. This difference is called the error vector. Figure 2.1 shows a graphical representation of its calculation. The PA distortion measurement can be simplified by using the EVM. It possesses a direct relationship with the signal-to-noise and distortion ratio (SNDR), and can be used to determine the physical error introduced at different stages of a communication system.

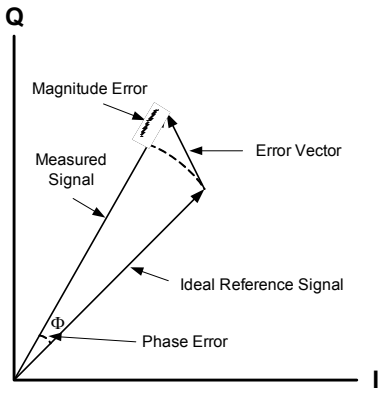


Figure 2.1 Error vector magnitude.

Figure 2.2 illustrates the EVM calculation mechanism in a VSA. The EVM can be calculated by regenerating an ideal, noise-free version of the input signal, and subtracting it from the original in order to obtain the error vector signal that includes residual noise and distortion.

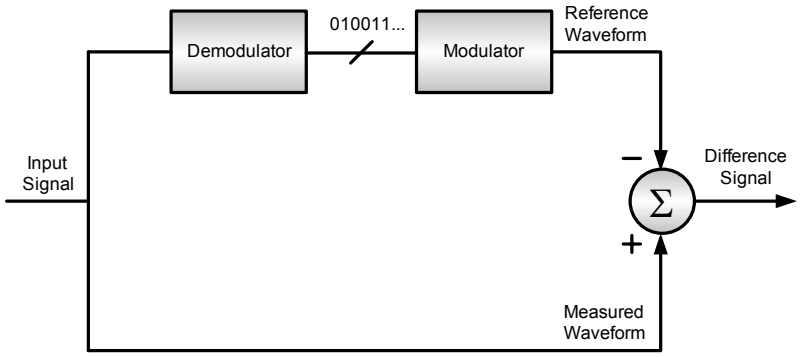


Figure 2.2 EVM calculation mechanism in a vector signal analyzer.

2.3 SYSTEM ARCHITECTURE

Figure 2.3 describes the adaptive digital predistortion system. Digital predistortion algorithms are often adaptive because the distortion characteristics of a PA may change

slowly over the operational power level, supply voltage, temperature and other conditions. The adaptation process is based on an EVM measurement of PA output signals. Using such EVM information, baseband I/Q waveforms may be corrected (predistorted) in subsequent symbols.

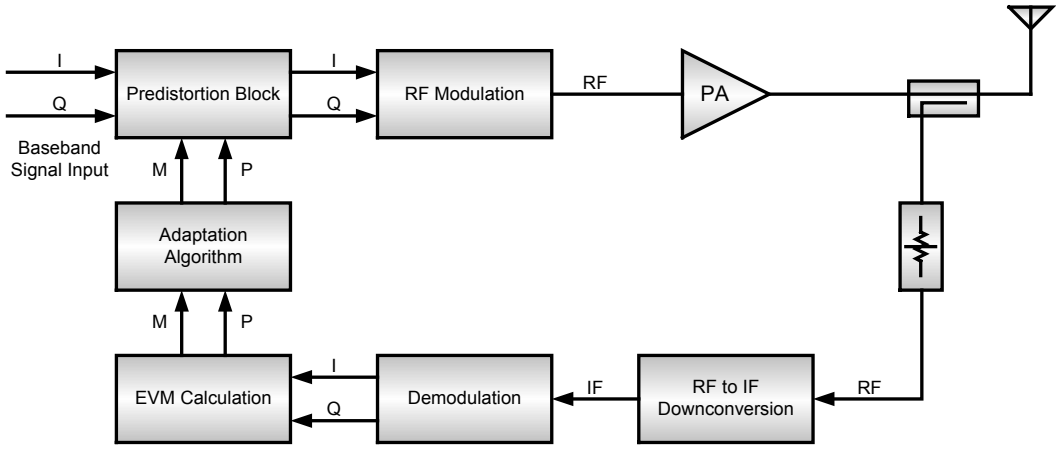


Figure 2.3 Block diagram of the adaptive digital predistortion.

2.4 ADAPTATION ALGORITHM

A program for adaptive digital predistortion was developed to operate in conjunction with the execution of the DSP-based predistortion algorithm, including all data collection from the PA. The predistortion algorithm uses two LUTs to adaptively characterize the inverse AM/AM and AM/PM responses of the PA. For each baseband input sample, the predistorted amplitude and phase signals are generated from the tables in conjunction with linear interpolation. The amplitude and phase tables are initialized to linear output and zero, respectively. Amplitude and phase errors are collected as a series of predistorted signals passes through the system. The correction values for the amplitude LUT, Δr, and for the phase LUT, $\Delta\theta$, are then generated by (2.2) and (2.3), respectively.

$$\Delta r = -\mu_r \cdot \frac{\varepsilon_r}{N}, \tag{2.2}$$

$$\Delta \theta = -\mu_\theta \cdot \frac{\varepsilon_\theta}{N}, \tag{2.3}$$

where μ_r and μ_θ are a constant to control the convergence rate and stability, ε_r and ε_θ are the amplitude and phase error correction value, and N is the total number of samples falling into the same slot in a LUT. Since the accumulation of correction values in a slot is affected by the frequency of samples appearing in the slot, N is used here to avoid an accumulation error.

For a given input baseband sample with amplitude falling into [n, n+1] of a table, the amplitude and phase tables are updated by the following equations:

$$r_{i+1}[n] = r_i[n] + \{1 - (k - n)\} \cdot \Delta r, \tag{2.4}$$

$$\theta_{i+1}[n] = \theta_i[n] + \{1 - (k - n)\} \cdot \Delta \theta, \tag{2.5}$$

where $r_i[n]$ and $\theta_i[n]$ correspond to the amplitude and phase table value in the slot n at the iteration i, respectively, and k is the input amplitude scaled to the table size. Also, n is the truncated integer value of k and is used as a LUT index. The linear interpolation equations (2.4) and (2.5) distribute the error correction values between slot n and n+1. At the end of the adaptation, a fourth-order polynomial is used to smooth the LUT function so that more spectrum improvement can be obtained with less iteration.

Although DSP codes for predistortion may be developed and evaluated independently from the RF PA, certain application issues make concurrent measurement necessary to produce really robust algorithms. One example is in choosing the correct size of a LUT for a particular PA that may amplify a number of different types of signals (i.e., in multimode

handsets). Another design consideration that must be made, in the design of both the algorithm and the PA, is the trade-off between linearity and efficiency. Finally, algorithms must be designed for stability, given the rate of change of the PA parameters. For example, the ACPR should not be significantly degraded when the power is changed. In modern cellular systems, such events occur often on a millisecond scale.

2.5 TEST SYSTEM IMPLEMENTATION

Figure 2.4 shows the diagram of the test system setup, which consists of a PC, an Agilent E4432B signal generator (SG), an Agilent E4404B spectrum analyzer (SA), an Agilent 89410A vector signal analyzer (VSA), and an Agilent 89411A downconverter.

In this test system, the PC operating under MATLAB creates quadrature phase shift keying (QPSK) I and Q signals for the pilot channel of a cdmaOne forward link signal. The signals created by the PC are modulated and upconverted to RF signals at an oversampling rate of up to 40 MHz. The limitation of the maximum available carrier frequency is dependent on the less available carrier frequency of the upconverter and the downconverter. Also, up to 3 GHz of carrier frequency can be on hand from the SG. This may easily be upconverted to 6 GHz with an external local oscillator (LO) and mixer. The E4404A and 89411A are utilized as a downconverter to frequency translate the amplified RF signal to the corresponding intermediate frequency (IF) signal. Since every device should be operated with the same clock for synchronization, the device with the best clock signal serves as the clock reference source for the other.

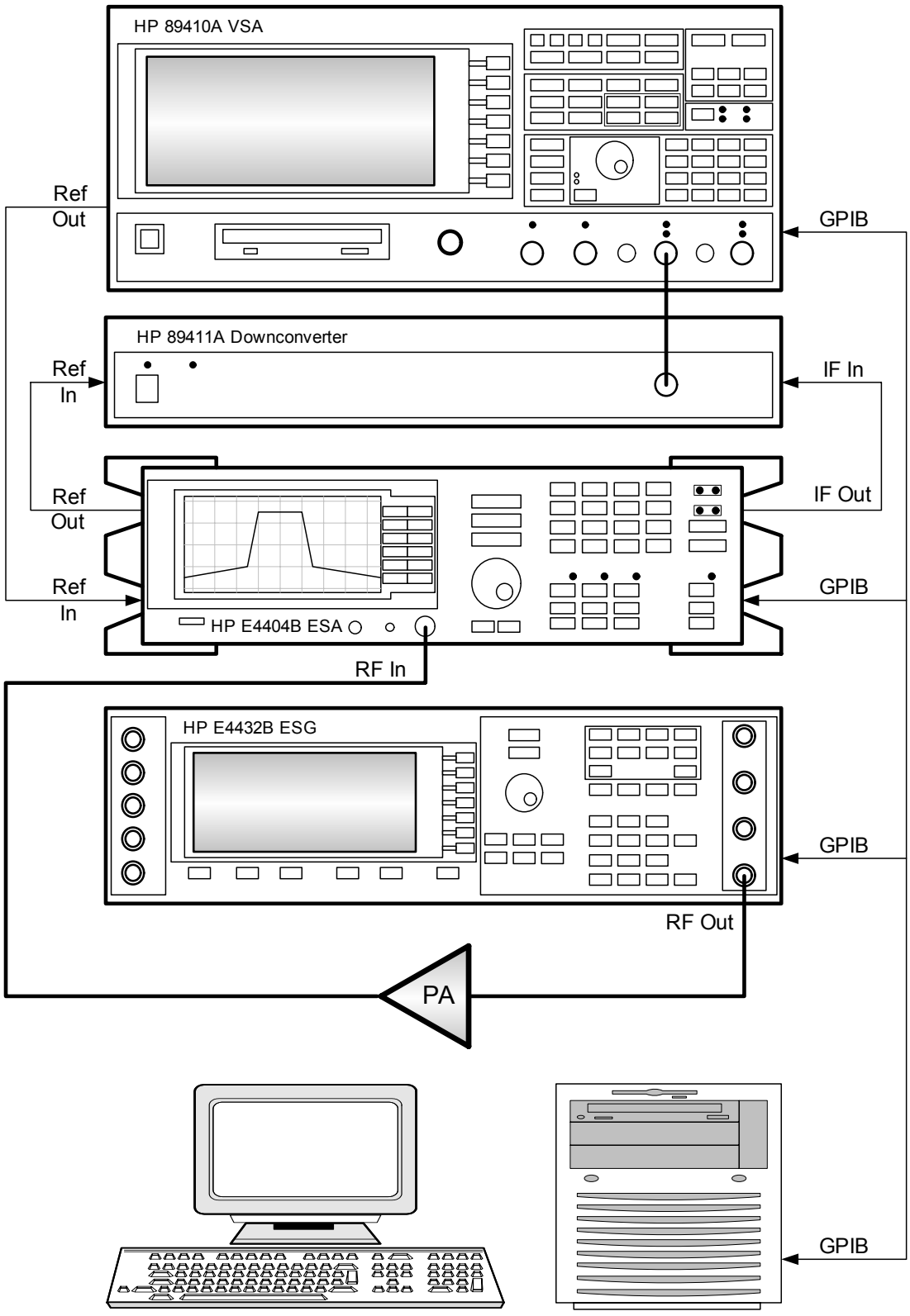
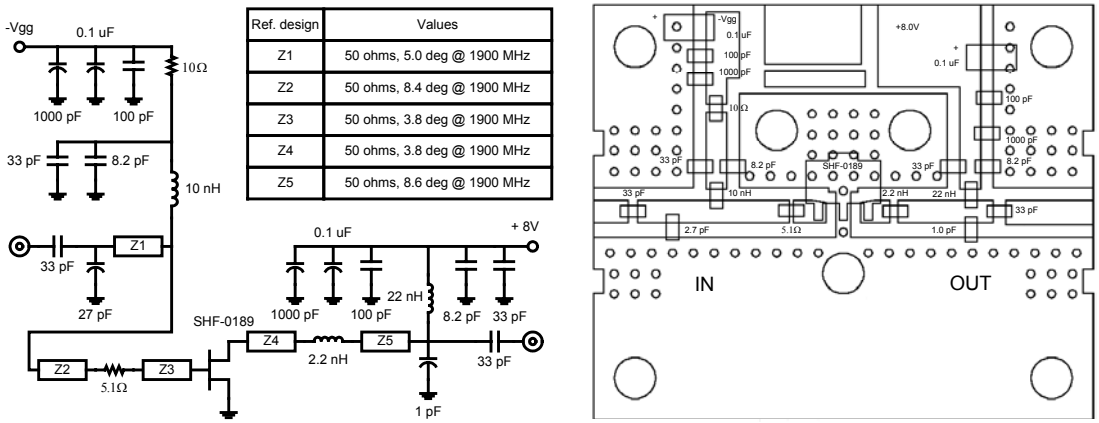


Figure 2.4 Test system setup for the adaptive digital predistortion.

2.6 EXPERIMENTAL RESULTS

The device under test (DUT) used in this experiment was a 0.5W GaAs/AlGaAs HFET PA (Sirenza SHF-0189). The nominal small signal gain was about 15.4 dB. The PA was biased with a quiescent drain current of 100 mA at 8 V_{DS} and –1 V_{GS}. Under these conditions, the output power at 1dB gain compression point (P_{1dB}) was measured to be 27.4 dBm. Figure 2.5 shows the schematic and printed circuit board (PCB) layout for the test circuit.



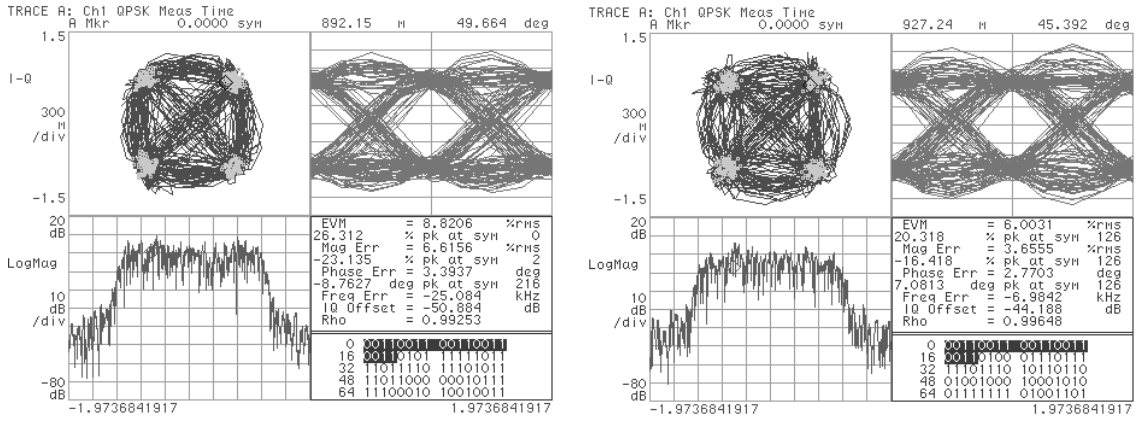
Ref. design	Values
Z1	50 ohms, 5.0 deg @ 1900 MHz
Z2	50 ohms, 8.4 deg @ 1900 MHz
Z3	50 ohms, 3.8 deg @ 1900 MHz
Z4	50 ohms, 3.8 deg @ 1900 MHz
Z5	50 ohms, 8.6 deg @ 1900 MHz

(a) (b)

Figure 2.5 0.5W PA (SHF-0189). (a) Schematic. (b) PCB layout.

The baseband signal used in this experiment follows the signal specifications of the TIA/EIA/IS-95B standard for the cdmaOne forward link transmitter. Its PAPR was about 9.5 dB.

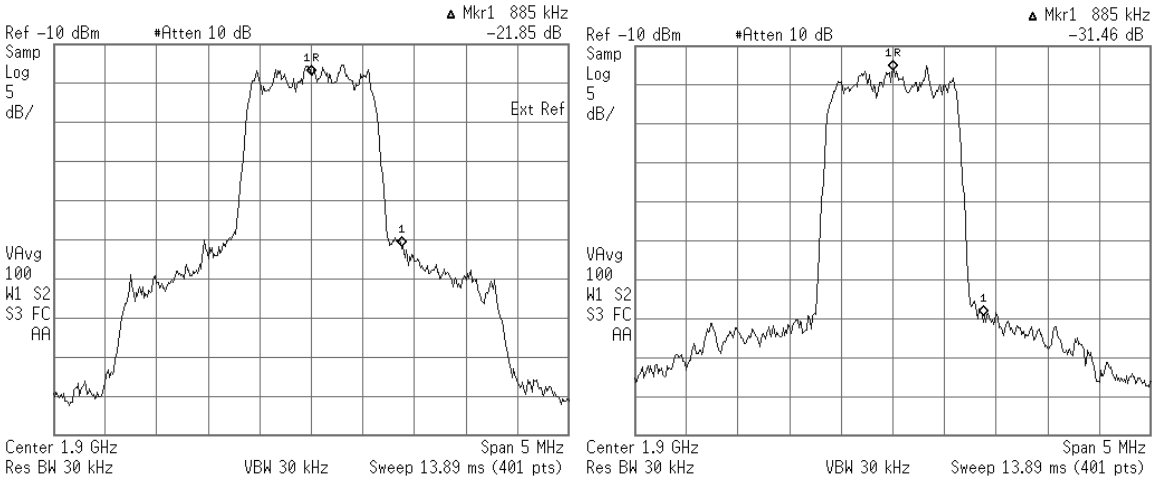
As shown in Figure 2.6, the EVM was improved by more than 2% after 10 iterations. The trajectories compressed before predistortion were significantly recovered after predistortion.



(a) (b)

Figure 2.6 EVM results of digital adaptive predistortion. (a) Before predistortion. (b) After predistortion.

Figure 2.7 displays the spectrum results that were obtained using a real-time DSP predistortion algorithm for the RF PA. As shown in Figure 2.7, the ACPR was improved by more than 9 dB after 10 iterations of the predistortion process. It was measured at a frequency offset of 885 kHz from the carrier frequency of 1.9 GHz.



(a) (b)

Figure 2.7 Spectrum results of digital adaptive predistortion. (a) Before predistortion. (b) After predistortion.

2.7 CONCLUSION

In this chapter, a baseband-to-baseband test system to characterize digital predistortion algorithms. This system used a digital adaptation method that was based on the error vector minimization of PA output waveforms. Using this system, an algorithm for memoryless baseband predistortion was tested in automated fashion and simulated the performance of a real-time DSP processor operating in conjunction with commercially available RF PAs.

CHAPTER III

HYBRID DIGITAL/RF ENVELOPE PREDISTORTION I - DESIGN AND SIMULATION

This chapter presents design and simulation methods for an adaptive wideband, digitally controlled RF envelope predistortion linearization system. A look-up table used for adaptation is indexed by a digitized envelope power signal and instantaneously adjusts the input signal amplitude and phase via an RF vector modulator to compensate for AM-AM and AM-PM distortion. The advantages of this hybrid digital/RF envelope predistortion architecture over conventional baseband digital approaches are that a 20-33% wider correction bandwidth is achievable at the same clock speeds, and linearization can be performed without the need for a digital baseband input signal. Therefore, this architecture can be used for repeaters as well as in existing 2G base stations. The timing match issue between the input RF signal and the predistorting signal, which is one of the critical factors for performance, is investigated as a way to achieve optimum performance.

3.1 INTRODUCTION

The enormous expansion of mobile phone subscribers and multimedia services in modern communications drives the capacity and flexibility increases of PAs in base station transmitters and leads to multicarrier operation. The hybrid RF envelope predistortion architecture discussed in this chapter provides a compromise between analog RF

predistortion and baseband digital predistortion. The predistortion technique provides wideband operation in that the bandwidth is not limited by DSP computational speeds because the signal manipulation is done directly on the RF signal under the control of high-speed digital circuits. The primary disadvantage of the hybrid predistortion system is its limited ability to correct memory effects that occur within the RF bandwidth. Frequency response can be a cause of such RF memory effects. This same limitation is present in feed-forward correction systems. However, techniques have been developed for narrowband PAs so that RF frequency response is rarely the limiting factor in digital predistortion systems [2]. Envelope memory effects, such as thermal feedback and baseband termination effects due to non-ideal bias circuit performance are more dominant in determining the limitations of memoryless predistortion systems [32].

To the best of the author's knowledge, the first fully adaptive envelope predistortion system architecture was demonstrated by Rey in [27]. An adaptive polar analog work-function predistortion system was employed to get a correction of about 20 dB for a 1.2 MHz bandwidth CDMA signal in the third-order IMD region, but only achieved up to 7 dB improvement for a wideband two-carrier test at 10 MHz spacing. A more advanced predistortion architecture was discussed in [28] that used a digitally controlled I/Q vector modulator to predistort an RF input signal. However, because this architecture extracts the reference signal after the I/Q modulator, the nonlinear behavior of the modulator cannot be corrected. It achieved just 5 dB of ACPR correction for a WCDMA standard signal with a PAPR of 11.5 dB. Kusunoki *et al*. implemented a similar architecture for cellular phones based on polar envelope predistortion [29]. The system, however, was non-adaptive for AM-PM distortion and achieved only 6-7 dB of ACPR correction. Gentzler *et al*. also

patented a comparable architecture that uses analog circuits to extract PA characteristics [30]. In this case, the reference signal path must include a large delay to compensate for the long delay on the RF signal path. The advantages of this architecture over previously developed hybrid architectures are that more accurate and wider band operations may be obtained. These advantages are because this architecture is limited only by the LUT access time and not by DSP computational speed. In addition, the large delay compensation requirement in [30] is not a problem in the proposed architecture because errors from the delay mismatch can be corrected within the DSP algorithm.

In this chapter, a behavioral model-based multi-level mixed-signal design and simulation environment is presented that provides a solution at the system level to the problem of accurate modeling and simulation. This is achieved by partitioning the system into components that are modeled by schematic or analytic expressions at the behavioral level. This chapter also discusses timing mismatch effects between the input signal and predistorting signal.

3.2 HYBRID SYSTEM DESIGN

The design process must allow fast architectural optimization with explicit consideration of all architectural parameters. Otherwise, the critically important architecture area could not be covered systematically, which would have disastrous consequences for design time and quality. System designers know that they cannot fix an inefficient architecture at the circuit level. It will be proved quickly that no circuit tuner can compensate for it. Addressing this issue requires a clear definition of the architectural design area, including key parameters or variables. Parameterization on a block-by-block basis is most effective,

especially if a canonical design can be defined. Explicit definition of system objectives and constraints can then be defined and powerful optimization capabilities applied. The flow diagram shown in Figure 3.1 describes the hybrid or mixed-signal system design procedure. The hybrid system design begins with the definition of the system requirements and specifications. Computational performance and accuracy of the system-level simulations are directly related to the level of detail in the underlying block models.

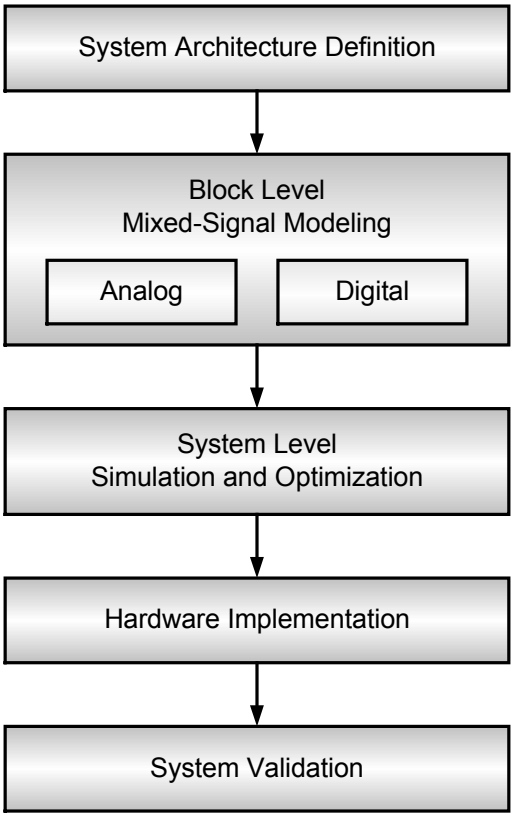


Figure 3.1 Hybrid digital/analog system design procedure.

3.3 SYSTEM ARCHITECTURE DEFINITION

Figure 3.2 describes the RF envelope predistortion system architecture. The operation of

this system is as follows: the EDET extracts the envelope of the input RF signal, which is then used as the index value for the LUT. The modulation signal from the LUT is then multiplied by the delayed input envelope signal in the VMOD to suppress the distortion at the output of the PA. The delay in the RF signal path is necessary to compensate for the processing and data conversion delay in the correction loop, which is formed by the EDET, LUT, and VMOD. Adaptation of the LUT is performed by sampling the signals at the input and output, demodulating them to obtain the complex envelopes, and calculating a least-squares best fit to minimize the predistortion function error. This process may be done off-line and does not require full Nyquist rate sampling [65].

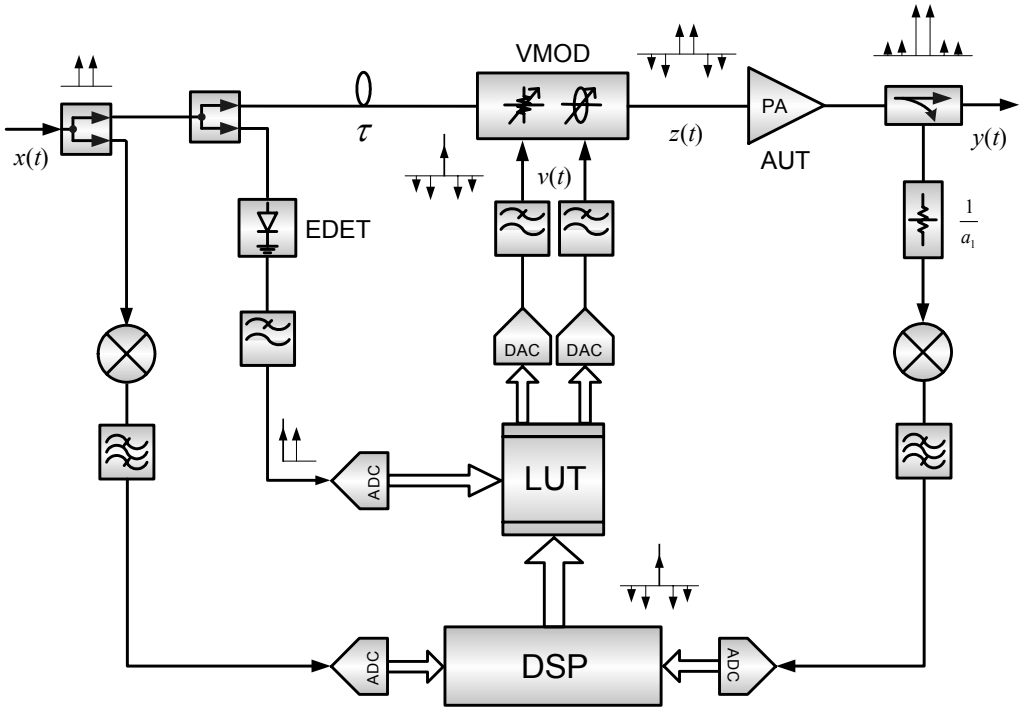


Figure 3.2 Block diagram of the RF envelope predistortion system.

3.4 MATHEMATICAL ANALYSIS OF THE EPD SYSTEM OPERATION

An analysis of the hybrid envelope predistortion is presented in this section. Suppose an equal power two-tone input signal $x(t)$ is defined by

$$\begin{aligned} x(t) &= \mathrm{Re}\left\{ Ae^{j\omega_1 t} + Ae^{j\omega_2 t} \right\} \\ &= \mathrm{Re}\left\{ \tilde{x}(t) \cdot e^{j\omega_c t} \right\} \end{aligned}, \tag{3.1}$$

where A is the amplitude of the input signals, $\tilde{x}(t)$ is the complex envelope of the input signal, and ω_c is the carrier frequency in radian/sec. The magnitude $|\tilde{x}(t)|$ of the two-tone input signal envelope, which is extracted by the EDET, can be described as

$$\left|\tilde{x}(t)\right| = \sqrt{\frac{1}{2}\left\{1 + \cos\left[(\omega_2 - \omega_1)t\right]\right\}}, \tag{3.2}$$

where A has been normalized to unity.

For simplicity, assuming that the odd order intermodulation terms up to the fifth order are dominant and that the PA is memoryless, the output $y(t)$ of the amplifier is given as

$$\begin{aligned} y(t) &= x(t) \cdot \sum_{k=1}^{3} a_{2k-1} \cdot \left| x^{2(k-1)}(t) \right| \\ &= a_1 \cdot x(t) + a_3 \cdot x^3(t) + a_5 \cdot x^5(t) \end{aligned}, \tag{3.3}$$

where $a_{2k\text{-}1}$ is the complex coefficient.

For the LUT adaptation, the baseband signals are extracted after the RF signals have been downconverted and sampled. They are then processed to identify the nonlinear characteristics of the PA in the digital signal processor. With (3.3) normalized by the linear gain, the i^{th} sequence of the discrete error signal, $\mathbf{e}_i$, can be written as

$$\begin{aligned}\mathbf{e}_i &= 1 - \frac{\mathbf{y}_i}{a_1 \cdot \mathbf{x}_i} \\ &= -\left(\frac{a_3}{a_1} \cdot |\mathbf{x}_i|^2 + \frac{a_5}{a_1} \cdot |\mathbf{x}_i|^4 \right),\end{aligned} \tag{3.4}$$

where $\mathbf{e}_i=[e_i(0), \cdots, e_i(N\text{-}1)]^T$, $\mathbf{x}_i=[x_i(0), \cdots, x_i(N\text{-}1)]^T$, $\mathbf{y}_i=[y_i(0), \cdots, y_i(N\text{-}1)]^T$, and N is the number of samples.

The result is used for updating the LUT adaptively by using a *least mean square* (LMS) algorithm. After i iterations, we can get the following equation:

$$\begin{aligned}\mathbf{LUT}_{i+1}\{|\mathbf{x}_i|\} &= \mathbf{LUT}_i\{|\mathbf{x}_i|\} + \mu \cdot \mathbf{e}_i \\ &= \mathbf{LUT}_i\{|\mathbf{x}_i|\} - \mu \cdot \left(\frac{a_3}{a_1} \cdot |\mathbf{x}_i|^2 + \frac{a_5}{a_1} \cdot |\mathbf{x}_i|^4 \right), \\ &= \mathbf{LUT}_i\{|\mathbf{x}_i|\} - b_3 \cdot |\mathbf{x}_i|^2 - b_5 \cdot |\mathbf{x}_i|^4\end{aligned} \tag{3.5}$$

where $\mathbf{LUT}_i=[lut_i(0), \cdots, lut_i(L\text{-}1)]^T$, L is the LUT size, μ is the stability factor, and $b_{2k\text{-}1}$ is the complex coefficient.

Assuming that the LUT is initialized by a constant b_1, and the first iteration has been performed, the predistorting signal $v(t)$ from the LUT through the DAC and reconstruction filter is a function of the index value $|\tilde{x}(t)|$, and is described as

$$\begin{aligned}v\{|\tilde{x}(t)|\} &= v_I\{|\tilde{x}(t)|\} + iv_Q\{|\tilde{x}(t)|\} \\ &= b_1 - b_3 \cdot |\tilde{x}(t)|^2 - b_5 \cdot |\tilde{x}(t)|^4 \\ &= \left(b_1 - \frac{b_3}{2} - \frac{3b_5}{8} \right) - \frac{b_3 + b_5}{2} \cos[(\omega_2 - \omega_1)t] - \frac{b_5}{8} \cos[2(\omega_2 - \omega_1)t]\end{aligned}, \tag{3.6}$$

where $v_I(t)$ and $v_Q(t)$ are the control signals for the I and Q branch of the VMOD, respectively. The constant term controls the gain of the PA. It does not control the intermodulation products, but becomes fairly significant when an amplifier such as a class

AB PA produces distortion at low input power levels. In addition, it is seen from (3.6) that the cutoff frequency of the reconstruction filter should be at least two times the input signal bandwidth to compensate for IMD products of up to the fifth order.

The predistortion function $z(t)$ is generated by the multiplication of the input signal $x(t)$ and the predistorting signal $v(t)$ from the LUT as follows:

$$\begin{aligned} z(t) &= x(t) \cdot v(t) \\ &= \beta_0 \cdot \{\cos(\omega_1 t) + \cos(\omega_2 t)\} \\ &\quad - \beta_1 \cdot \{\cos[(2\omega_1 - \omega_2)t] + \cos[(2\omega_2 - \omega_1)t]\} \\ &\quad - \beta_2 \cdot \{\cos[(3\omega_1 - 2\omega_2)t] + \cos[(3\omega_2 - 2\omega_1)t]\} \end{aligned} \quad . \tag{3.7}$$

From the proper selection of the coefficients β_k by the iterative adaptation, these predistorting terms are used to reduce the third- and fifth-order IMD products generated by the PA.

3.5 MIXED-SIGNAL MODELS

The predistortion system consists of mixed-signal circuits and subsystems. Simulation of RF and digital signals has been problematic in that RF components are generally simulated in the frequency domain at circuit level, whereas the digital subsystem is simulated behaviorally in the time domain. Moreover, increasing system complexity, reduced size, and decreasing time-to-market drive the need for full system-level simulation and optimization [66]. Behavioral modeling of RF components has been proposed as a way to bridge the gap to do full system simulation [67], [68]. This section presents a mixed-signal behavioral simulation of the envelope predistortion system. The behavioral technique allows for trade-offs to be made between the digital subsystem and the RF component

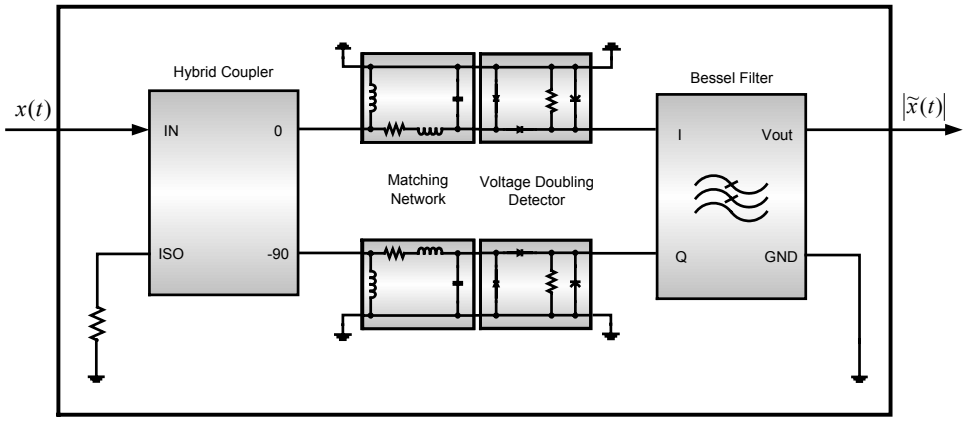
design so as to optimize system performance.

Mixed-signal system models were developed using an Agilent ADS™. They include frequency-dependent models in time domain simulation. The RF components such as the VMOD and EDET were modeled by using microstrip lines based on the transmission line theory. After RF signals are converted into digital signals, they are used by the digital components such as arithmetic components and random access memories (RAMs) that are employed in a LUT.

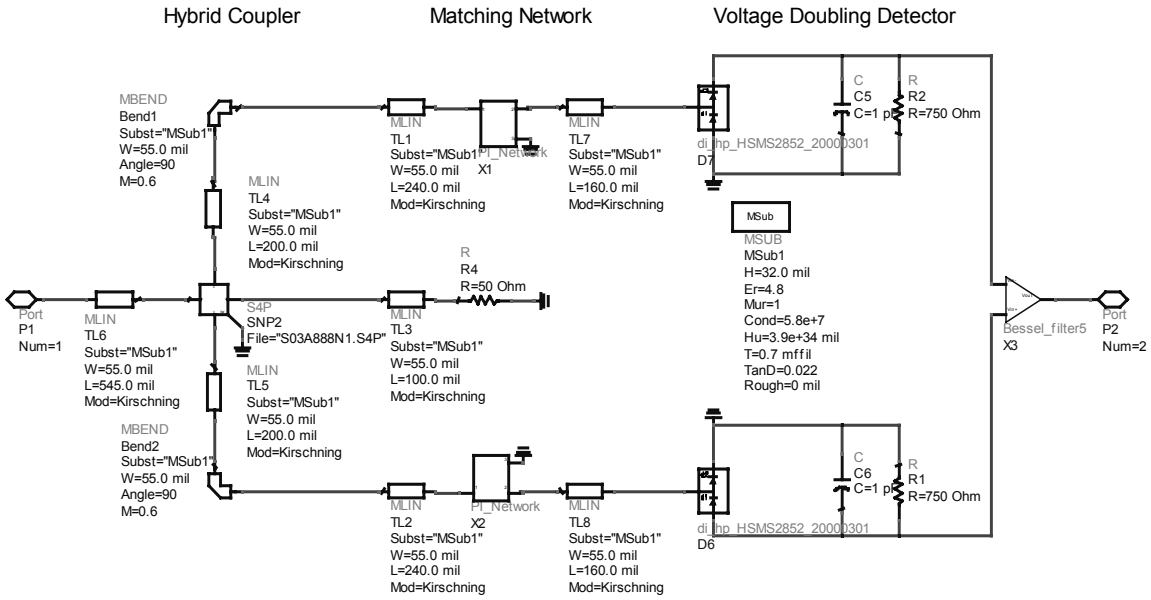
3.5.1 Envelope Detector Simulation Model

Figure 3.3 shows the RF envelope detector (EDET) used for the system to monitor signal amplitude and index the LUT. A balanced configuration with matching networks provides a good voltage standing wave ratio (VSWR) and low reverse IMD. Also, the matching network provides the minimum return loss for the diode detector. A 90° hybrid coupler is employed to minimize the reflected odd harmonics. The voltage-doubling detector gives twice the voltage level that a single diode detector can provide. The Bessel lowpass filter (LPF) with the normalized transfer function $H(s)$ in (3.8) removes aliasing signals and unwanted harmonic frequencies, allowing a flat group delay in a wide range.

$$H(s) = \frac{1}{0.591 \cdot s^3 + 1.764 \cdot s^2 + 2.318 \cdot s + 1}. \tag{3.8}$$



(a)



(b)

Figure 3.3 EDET simulation model. (a) Block diagram. (b) Schematic.

Figure 3.4 shows the simulation results obtained from the EDET model. The EDET exhibits a square-law characteristic over a range of input powers up to –5 dBm. Because of the wideband impedance matching used in the design, the EDET responses at 869 MHz and 894 MHz show difference of up to 0.3 dB.

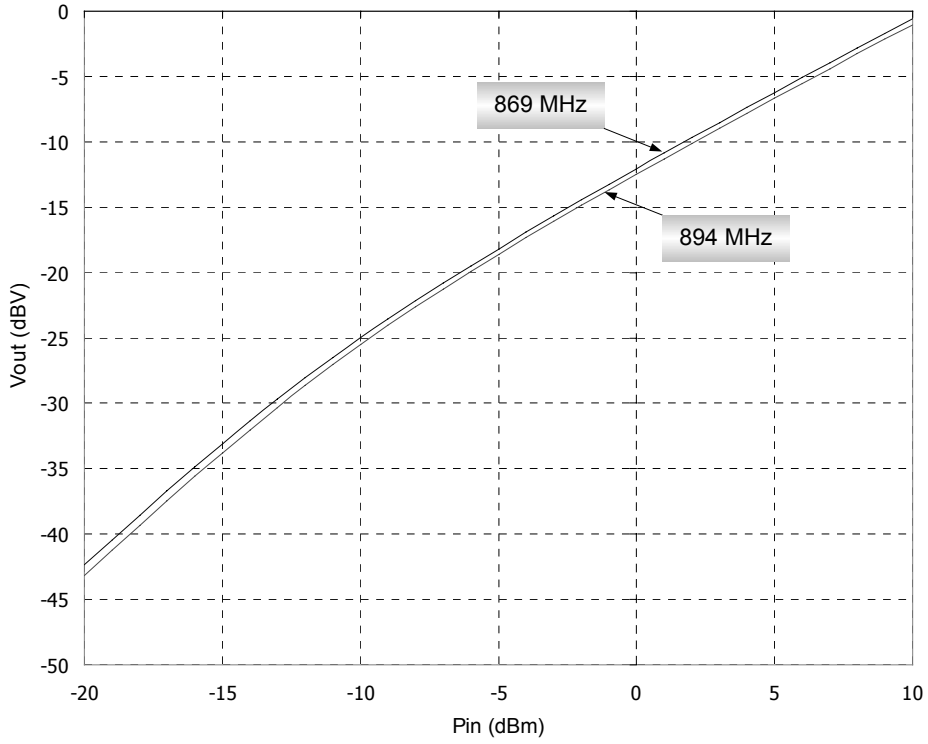
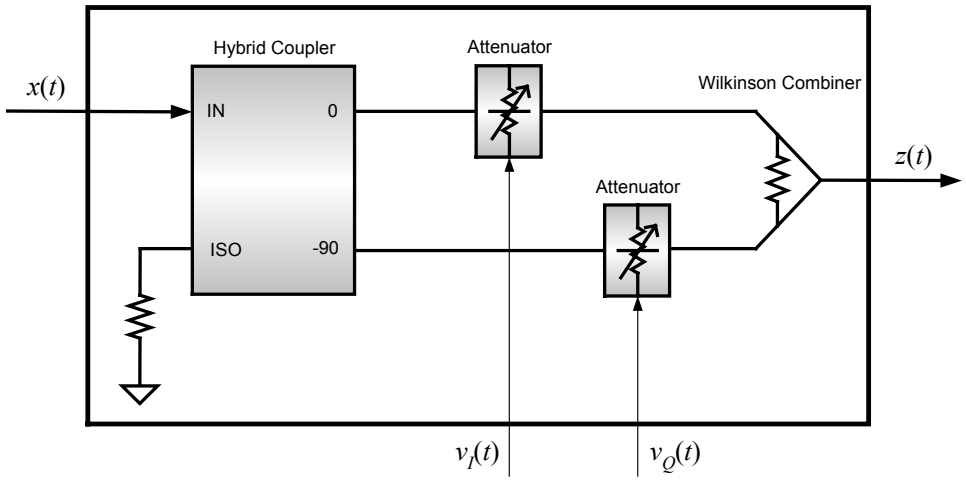


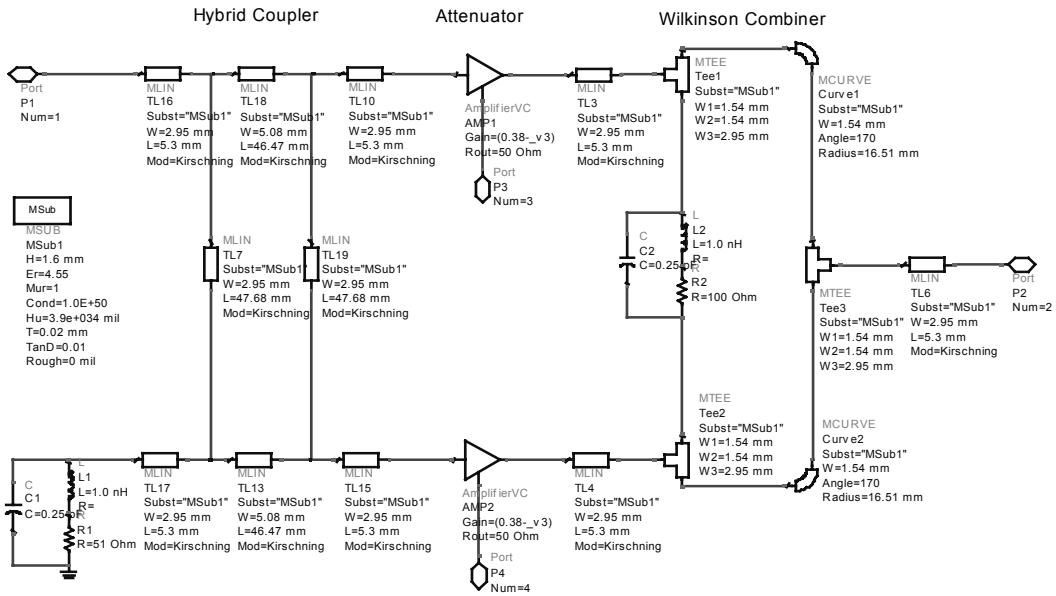
Figure 3.4 Simulated output voltage response of the EDET to the input power.

3.5.2 Vector Modulator Simulation Model

The most common method for vector modulator (VMOD) implementation is to use variable attenuators that operate on quadrature signals to produce the desired amplitude and phase values when they are summed. The VMOD shown in Figure 3.5 consists of a 90° hybrid coupler, two variable attenuators, and a Wilkinson combiner. Each of the I and Q signal is attenuated by the modulating signals, which come from the LUTs through the digital-to-analog converters (DACs).



(a)



(b)

Figure 3.5 VMOD simulation model. (a) Block diagram. (b) Schematic.

The simulation results obtained from the VMOD model are shown in Figure 3.6. Comparing the vector-modulation dynamic ranges simulated at 869 MHz and at 894 MHz, it displays differences of up to 0.25 dB in gain and 10.8° in phase.

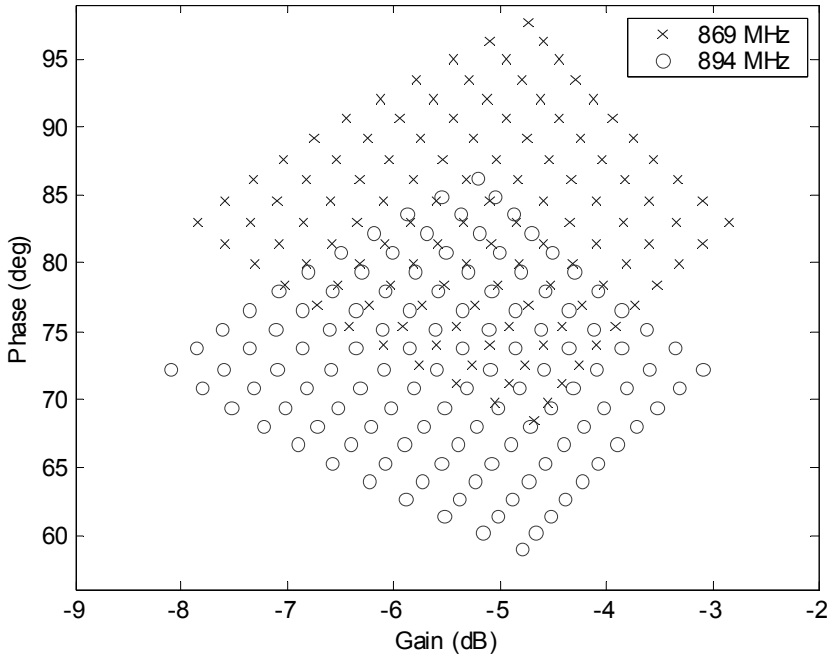


Figure 3.6 Simulated VMOD dynamic range.

3.5.3 Digital Signal Processing Model

Figure 3.7 shows the DSP module in which the LUT adaptation is performed. In the LUT adaptation, the envelopes are extracted after the RF signals are downconverted and sampled. Then, they are processed to identify the nonlinear characteristics of the PA in the DSP. The results are used to update the LUT adaptively based on the LMS algorithm that is described in 3.4. The adaptive work function (AWF) performs comparison of the input reference signal and the PA output signal to obtain complex gain errors. This process is also described in 3.4.

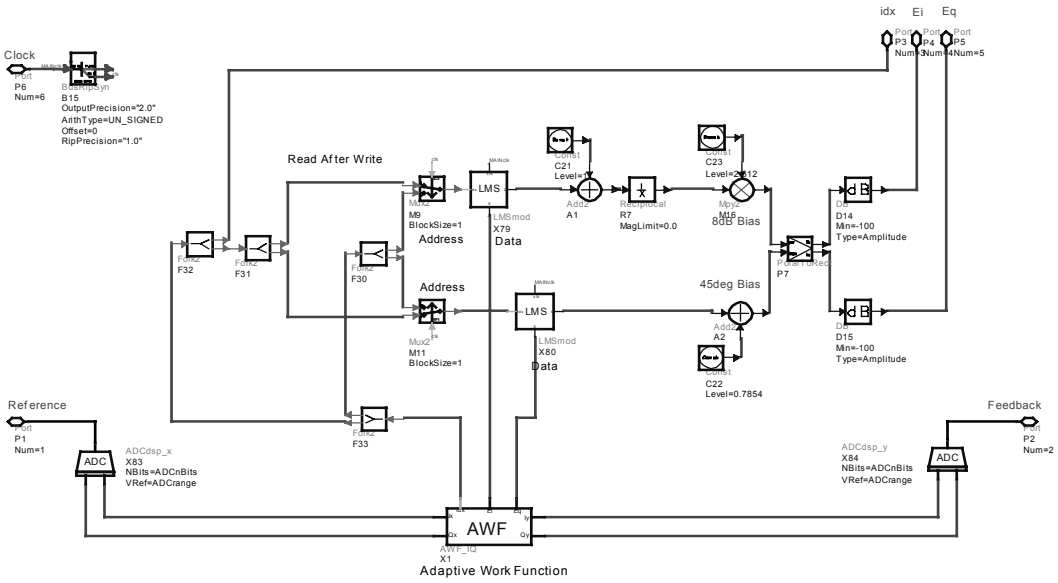


Figure 3.7 Schematic of the adaptive digital signal processing model.

Figure 3.8 illustrates the LUT adaptation behavior. As values in the gain LUT are adaptively changed by the information from the DSP module, the AM/AM nonlinear characteristic of the PA becomes linear.

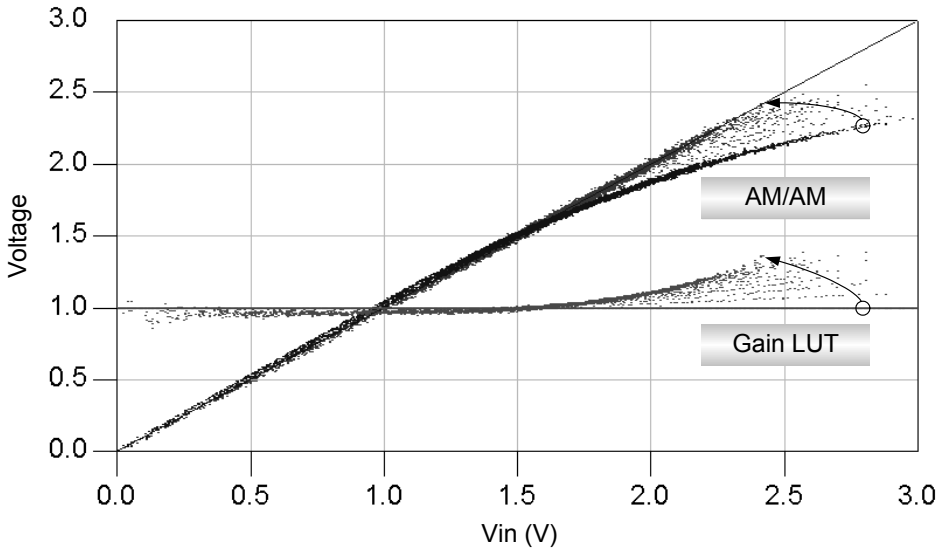


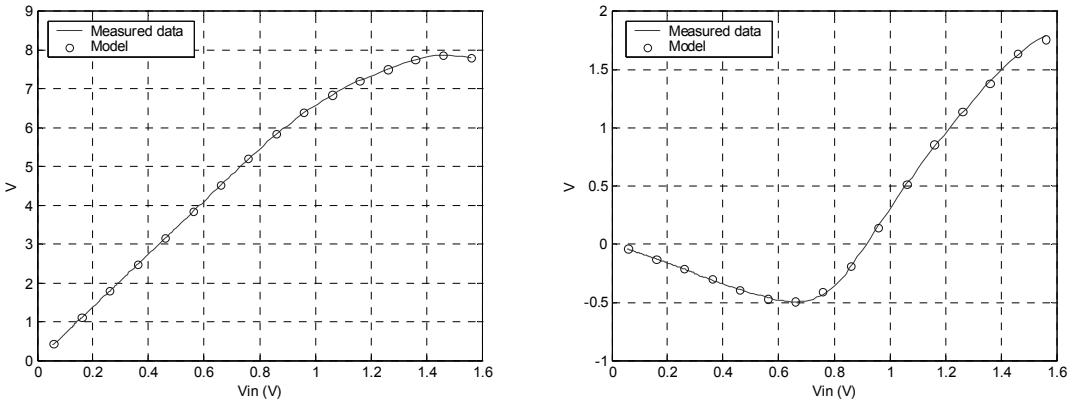
Figure 3.8 Simulated LUT adaptation operation by using the DSP module.

3.5.4 Power Amplifier Simulation Model

In this simulation, the amplifier tested was the Sirenza 0.5W HFET PA (SHF-0189). A behavioral model of the PA was extracted at 881.5 MHz by fitting the AM-AM and AM-PM distortion functions to ninth-order polynomials, as shown in Table 3.1. Figure 3.9 indicates that the PA model agrees well with the measured data. The output power at 1dB gain compression point (P_{1dB}) was 27 dBm in the simulation.

Table 3.1 PA model coefficients.

	x^0	x^1	x^2	x^3	x^4	x^5	x^6	x^7	x^8	x^9
I	-0.01	7.25	-6.18	43.96	-164.39	340.97	-402.25	266.59	-92.43	13.04
Q	-0.02	0.1	-10.89	53.92	-126.78	124.89	3.73	-94.15	62.30	-12.82



(a) (b)

Figure 3.9 PA model used in the simulation. (a) In-phase (I). (b) Quadrature-phase (Q).

3.6 SYSTEM-LEVEL SIMULATION AND OPTIMIZATION

3.6.1 Optimum Resolution of the Signal Converters

The optimum values of ADCs and DACs were determined based on the simulation results shown in Figure 3.10.

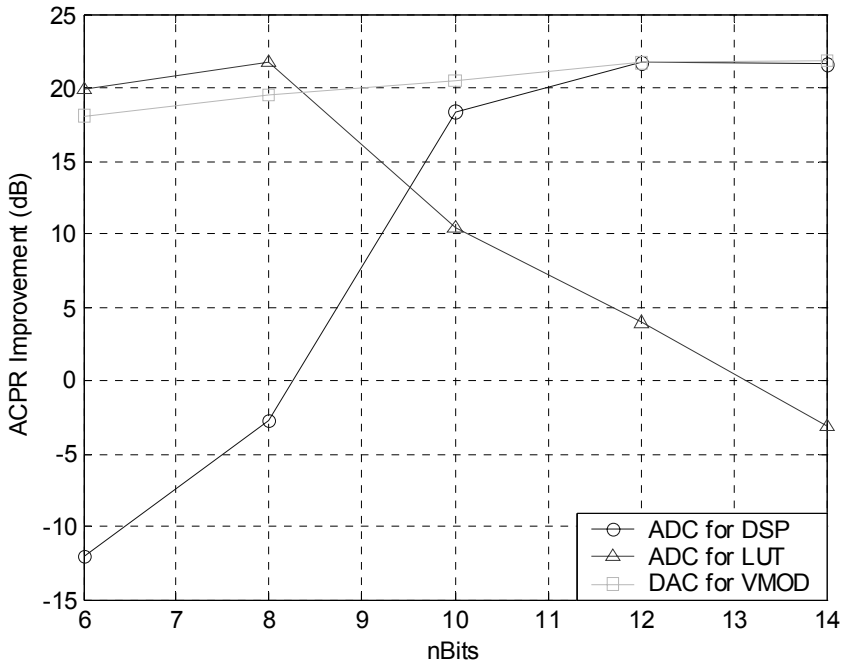


Figure 3.10 Optimum resolutions for ADC and DAC.

As shown in Figure 3.10, the optimum resolutions of the ADC for indexing the LUT, the DAC for controlling the VMOD, and the ADC for the DSP were determined to be 10 bits, 12 bits, and 14 bits, respectively, considering the degradation of 1.5 least significant bits (LSBs) in terms of signal-to-noise ratio (SNR) [69]. The resolution of the ADC for the LUT indexing should be taken into consideration because the update rate to a specific LUT

entry depends on the resolution of the ADC. On the other hand, because the ADC for the DSP is on the iterative adaptation loop, its resolution should be as high as possible. Because of the nonlinear characteristics loaded in the LUT, the DAC should have a resolution higher than the ADC.

3.6.2 Optimum Sampling Frequency on the Correction Loop

Figure 3.11 shows the simulated performance of the predistortion system and the sampling frequency requirement for the ADC/DAC. Spectra (a) and (c) indicate that the sampling frequency must be at least four times the input signal bandwidth to deal with third- and fifth-order spectral regrowth and achieve linearization. As shown in (b) and (c), about 20 dB improvement in ACPR was obtained with 4X oversampling, an LUT size of 256 words, and a 12-bit DAC.

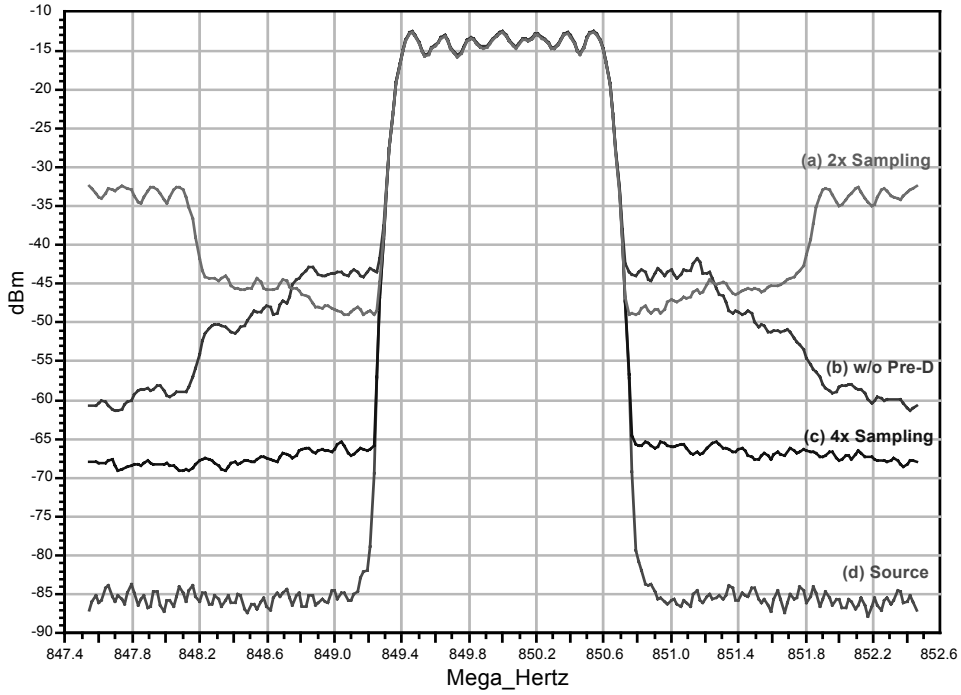


Figure 3.11 Spectrum results for the sampling frequency requirement.

3.6.3 Timing Mismatch Effects

Figure 3.12 describes the delay time relationship in the RF predistortion. The VMOD is operated by the vector signal (predistorting signal) from the control function $L(\cdot)$, based on the input signal envelope. Therefore, the delay of the input RF signal $x(t)$ must be matched accurately to the delay of the predistorting signal $v(t)$ in the VMOD. The accuracy of this match is a critical factor in achieving high linearization performance within the hybrid predistortion approach.

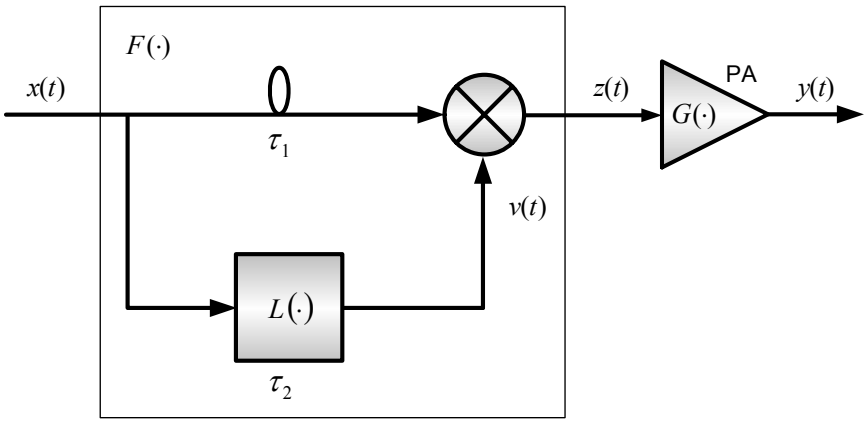


Figure 3.12 Block diagram of the RF predistortion function.

The predistortion linearized output $y(t)$ in terms of timing mismatch can be described by the following equations:

$$\begin{aligned} y(t) &= G[z(t)] = G[F(x(t))] \\ &= \mathrm{Re}\left\{ g\left[\left|F(x(t))\right|\right] \cdot e^{j\left\{\psi\left[\left|x(t-\tau_1)\right|\right] + \theta\left[\left|F(x(t))\right|\right]\right\}} \right\}, \end{aligned} \tag{3.9}$$

$$F(x(t)) = x(t-\tau_1) \cdot L\left[\left|x(t-\tau_2)\right|\right], \tag{3.10}$$

where $g(\cdot)$ and $\theta(\cdot)$ are the amplitude and phase response function of the PA, respectively, and $\psi(\cdot)$ is the phase response function of the predistortion function $F(\cdot)$.

Figure 3.13 shows the simulation and measurement results for the delay mismatch (τ_2-τ_1) when two-tone signals with tone spacing of 2 MHz and 3 MHz are used. Two-tone signal analysis is used for simplicity to provide an estimate of the effects of the delay mismatch. Using a least-squares fitting method, the PA model $G(\cdot)$ and predistorting function $F(\cdot)$ for the simulation were extracted from the calibration system, which was studied in [57].

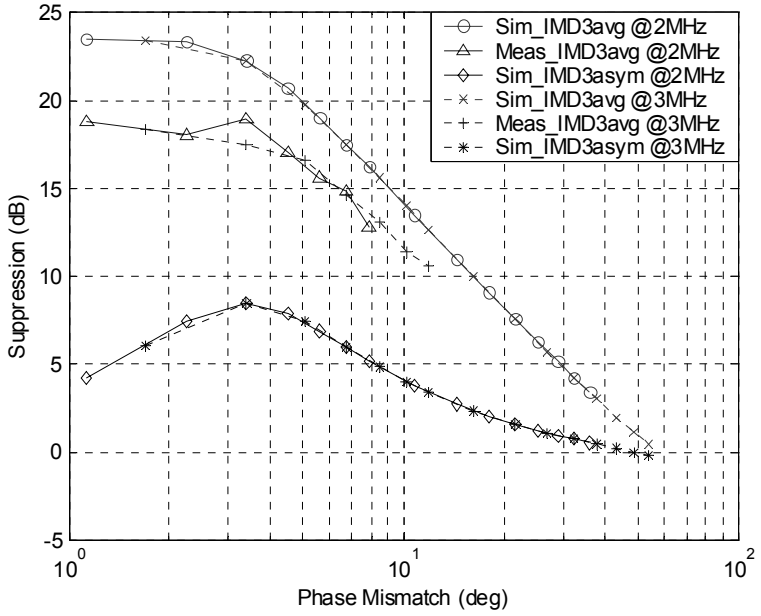


Figure 3.13 IMD3 suppression vs. phase mismatch.

The asymptotic slopes for the IMD suppression of the measured results agree well with those from the simulation, although there is around a 3 dB difference. The discrepancies at low levels are caused by amplitude mismatches or by other system errors in the setup. The IMD suppression decreases mildly until a phase offset of around 4°, which means that in this range the phase error is negligible compared with the amplitude error in this range. The largest asymmetry was found at a phase offset of 3.4° from the matching point. According

to Figure 3.13, the degradation of IMD suppression in dB over the phase error, Ψ, can be described by

$$\Psi = -20\log_{10}\left|\varepsilon_{\theta}\right|, \tag{3.11}$$

where ε_{θ} is the phase error in degrees. Equation (3.11) implies that the degradation is inversely proportional to the square of the phase error [34].

3.7 CONCLUSION

In this chapter, an RF envelope predistortion linearization system for PAs was discussed. The architecture described in this chapter employs an FPGA-based look-up table that controls a high-speed VMOD. By controlling the VMOD in response to the RF envelope level, the PA is linearized to the extent that memoryless predistortion is possible. A mixed-signal behavioral simulation system for PA predistortion was developed using an Agilent ADS™ computer-aided design system. Behavioral models were extracted from the RF components and simulated in the same file with the digital components. A look-up table was employed for adaptation and may be implemented in an FPGA for high-speed operation and design flexibility. Trade-offs are made between the FPGA design and the RF component designs to optimize the performance of the system. The system performs linearization for a physical model of a PA, which uses the dynamic feedback of the difference signal between the input and output envelope signal to adaptively compensate for the gain and phase. The effects of a timing mismatch between the input RF signal and the predistorting signal were investigated through the simulation and the experiment.

CHAPTER IV

HYBRID DIGITAL/RF ENVELOPE PREDISTORTION II - SYSTEM IMPLEMENTATION AND EXPERIMENTS

Chapter III consists of a discussion of the design and simulation methods for an adaptive wideband, digitally controlled RF envelope predistortion linearization system. This chapter describes in detail its implementation and methods of experimental verification.

4.1 INTRODUCTION

The predistortion technique described in this chapter employs a high-speed FPGA for the LUT that is slowly adapted based on time series samples to obtain maximum accuracy and consequent minimum distortion [58], [59]. In the predistortion architecture, the LUT automatically corrects nonlinearities in the EDET and RF VMOD control characteristics. Moreover, all timing control and data transfer are managed by the FPGA, which minimizes the computational load on the DSP.

The correction-loop test system was first implemented to verify the LUT-based correction-loop subsystem using a VNA, which was used as a PA characterization module. Using 3-carrier cdma2000 and multi-tone signals, the linearization performances for a 0.5W GaAs HFET PA and a 90W PEP LDMOS PA were examined on the test system.

The fully adaptive closed-loop envelope predistortion system was then implemented in combination of the correction-loop subsystem and the PA characterization subsystem.

Using 3-carrier cdmaOne and wideband multi-tone signals, the linearization performances for a 0.5W GaAs HFET PA, a 90W PEP LDMOS PA, and a 680W PEP LDMOS PA were examined. In addition, the predistortion performance variation for different signals was studied in terms of signal envelope statistics, output power, and PA power capacities.

4.2 HYBRID EPD SYSTEM DEVELOPMENT ENVIRONMENT

The block diagram shown in Figure 4.1 describes the development environment of the hybrid digital/RF envelope predistortion system. It can be classified into three portions: (a) software development (C/C++-based system management program and MATLAB-based predistortion function calculation program), (b) FPGA configuration design (VHDL-based LUT configuration design, Assembly-based microcontroller program, and ModelSim simulation), and (c) hardware development portion (correction-loop subsystem and characterization-loop subsystem). The system management program classified in the software development performs the DSP operation in conjunction with the MATLAB-based DSP algorithm and, through the GPIB connections, also controls operation of the test equipment. LUT configuration is designed in VHDL, verified by ModelSim simulation, and finally downloaded into an FPGA through the JTAG connection. LUT contents calculated by the DSP algorithm in a PC are updated into the FPGA through the RS232 or USB connection. The correction-loop subsystem for predistortion and the characterization-loop subsystem for RF-to-IF downconversion and data acquisition are included in the hardware development portion.

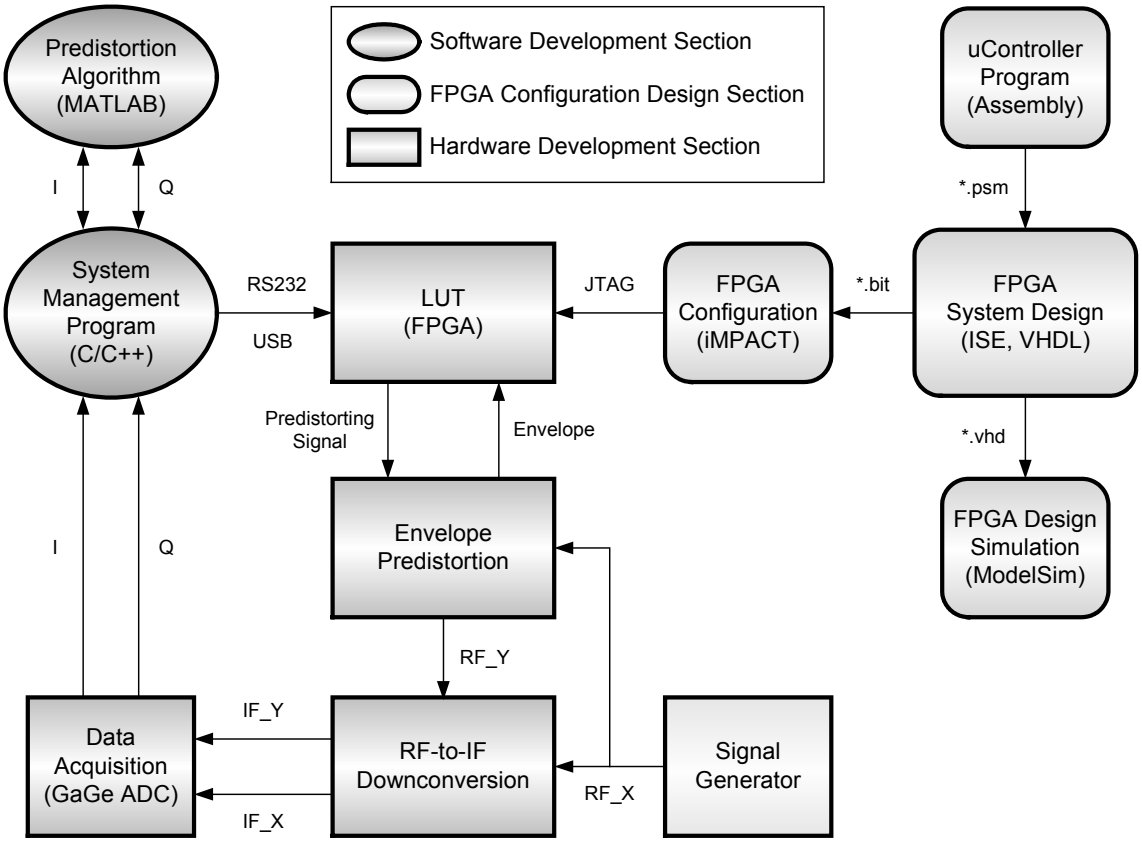


Figure 4.1 Implementation environment of the hybrid digital/RF envelope predistortion system.

4.3 PROTOTYPE IMPLEMENTATION OF THE HYBRID EPD SYSTEM

The prototype block diagram of the fully adaptive hybrid EPD system is shown in Figure 4.2. This system was implemented based on the theories and simulation results studied in Chapter III and consists of three large sections: (a) RF signal amplification, (b) a correction-loop subsystem, and (c)-(d) a characterization-loop subsystem. To avoid interference between the RF and digital signals, the correction-loop subsystem, which performs envelope predistortion, was housed separately from the PA characterization-loop subsystem. During the development of the system, its performance was found to be critically dependent on the integrity of the transmission of the high-speed digital signal.

Various experiments confirmed that crosstalk among high-speed digital buses could adversely affect the analog-to-digital conversion. As a result, care was taken to shield the ADC from digital noise and other interference. It was also determined that the ADC aperture jitter could severely degrade system performance. To reduce the aperture jitter, improvements were made to the phase noise of the oscillator driving the ADC.

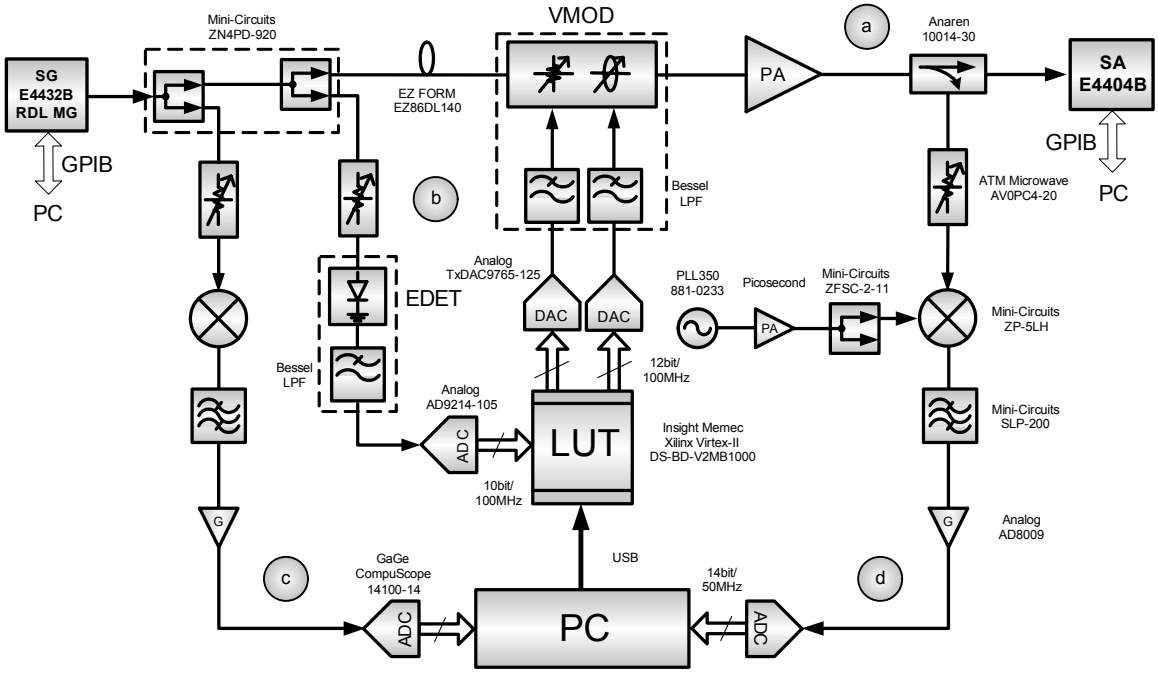
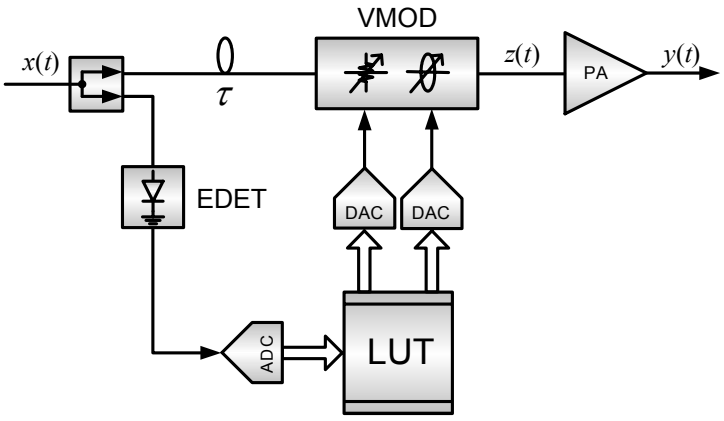


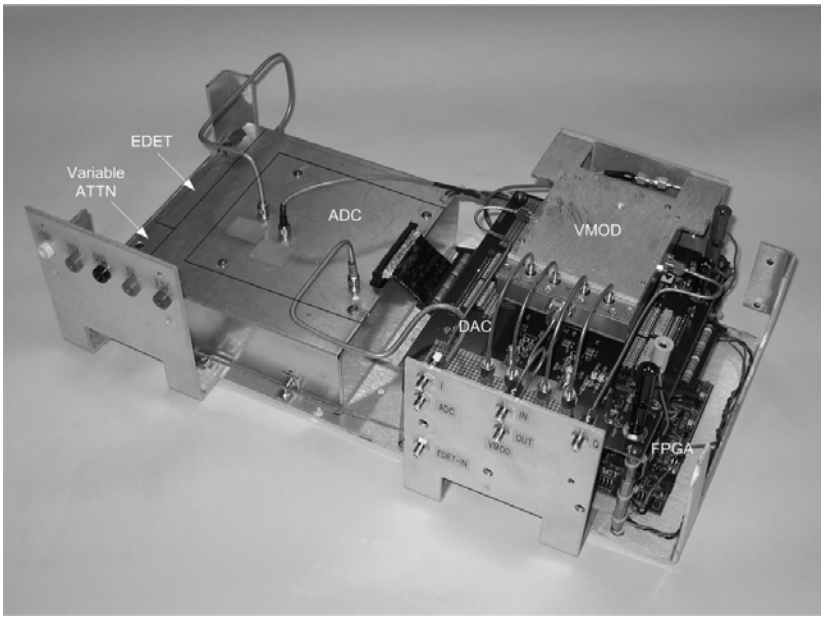
Figure 4.2 Details of the hybrid EPD system prototype. (a) RF signal amplification section. (b) Correction-loop subsystem section. (c)-(d) characterization-loop subsystem section.

4.4 CORRECTION-LOOP SUBSYSTEM

The correction-loop subsystem, which can be used as an independent open-loop predistortion system, includes mixed-signal modules: VMOD and EDET in analog and LUT in digital. Figure 4.3 shows the correction-loop subsystem that performs RF envelope predistortion using an FPGA LUT.



(a)



(b)

Figure 4.3 Correction-loop subsystem for the RF envelope predistortion. (a) Block diagram. (b) Prototype.

This mixed-signal subsystem permits more accurate and more wideband predistortion compared with predistortion techniques using only analog or digital approaches, although some degradation in signal-to-noise ratio (SNR) occurs because of the signal domain conversion in the use of the ADC/DAC.

The RF input signal $x(t)$ is predistorted before the main PA by the VMOD. The output signal $y(t)$ can be derived as

$$\begin{aligned} y(t) &= G\big(z(t)\big) = G\big[F\big(x(t)\big)\big] \\ &= \mathrm{Re}\Big\{g\big[f\big(|x(t)|\big)\big]\cdot e^{j\{\arg[x(t)]+\psi[|x(t)|]+\theta[f(|x(t)|)]\}}\Big\}, \end{aligned} \tag{4.1}$$

where $z(t)$ is the predistorted signal, and $G(\cdot)$ and $F(\cdot)$, respectively, are the complex nonlinear transfer function of the PA and predistortion circuit. Also, $g(\cdot)$ and $\theta(\cdot)$ are the amplitude and phase response functions of the PA, and $f(\cdot)$ and $\psi(\cdot)$, respectively, are the amplitude and phase response function of the predistortion circuit.

The VMOD modulates the input RF signal envelope based on the control values from the LUT. The delayed input envelope signal is then multiplied by the predistorting signal in the VMOD. In other words, this multiplication in the time domain means the convolution of the two signals in the frequency domain. Therefore, the correction-loop subsystem should have the capability to deal with the even-order bandwidth δB corresponding to the odd-order PA output distortion bandwidth $(1+\delta)B$ as in (4.2).

$$Z(f) = X(f) \otimes V(f) \;\Rightarrow\; B + \delta B = (1+\delta)B\,, \tag{4.2}$$

where $V(f)$ is the normalized complex signal of the inverse PA nonlinear characteristics in frequency domain, δ is an even integer, B is the envelope signal bandwidth, and $\otimes$ means convolution.

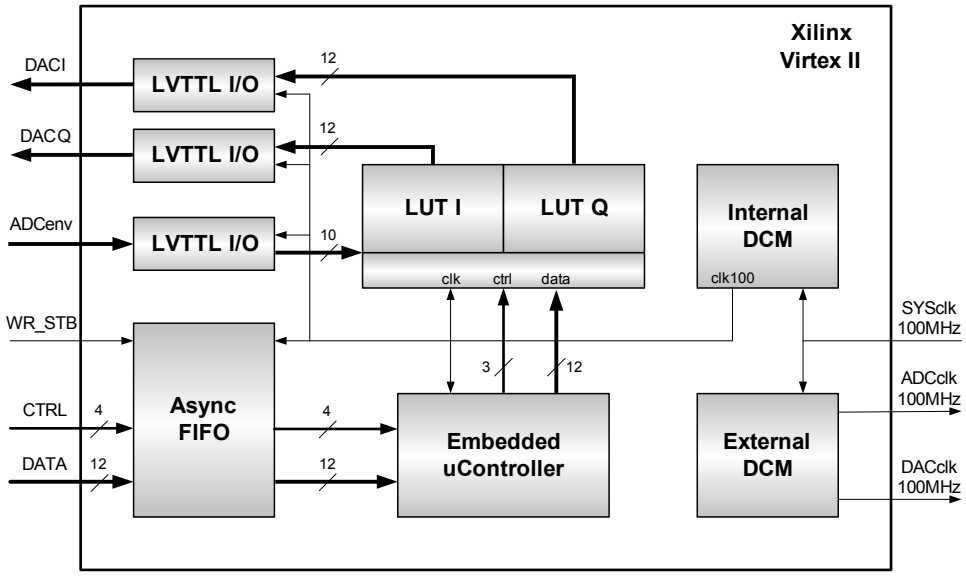
4.4.1 Look-Up Table

The LUT spacing strategy is one of the major concerns for system performance. There are different LUT spacing methods, such as equal spacing in amplitude or power, μ-law spacing, and optimum spacing [73]. The LUT used in this system has entries equally

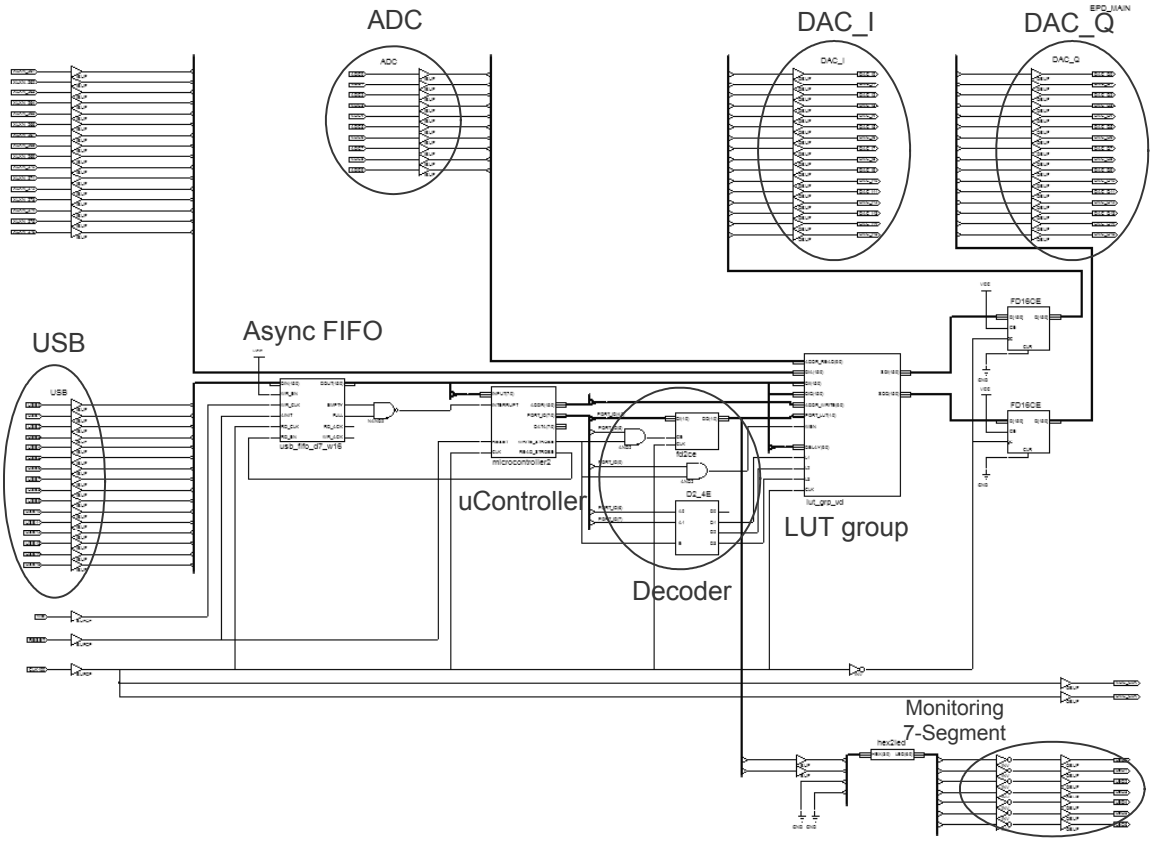
spaced in the input signal amplitude. As mentioned in [73], equispacing by amplitude offers many advantages such as operational simplicity and good performance without dependence on amplifiers, modulation format, etc.

Performance is the main objective in every aspect of designing complicated systems. Highest performance can be achieved when circuits are optimized for a single problem. New problems that require even minor changes require redesign and reoptimization of the entire system. Reconfigurable computing addresses this problem by allowing dedicated circuits to be built on to an FPGA. FPGAs provide a rapid prototyping platform that can be reprogrammed for different hardware functions without incurring the nonrecurring engineering costs typically associated with custom integrated circuit (IC) fabrication. This greatly improves system flexibility and functional density. Therefore, implementing LUT functions in an FPGA provides advantages over conventional hardware implementation: *Reconfigurability and Parallelism*.

By using a structure with a LUT separated from a DSP processor, the speed requirements of DSP are greatly reduced because it does not need to operate in real time. On the other hand, a high-speed operation is required in the LUT correction-loop subsystem so that it can be synchronized with the main signal path. A Xilinx Virtex-II FPGA was employed to implement the LUT. Its configuration shown in Figure 4.4 was designed to operate at 100 MHz clock speed. For the extended use of the LUT in the compensation for PA memory effects, each of the LUTI and LUTQ was designed to have 4 sub-LUTs with a corresponding programmable delay tap.



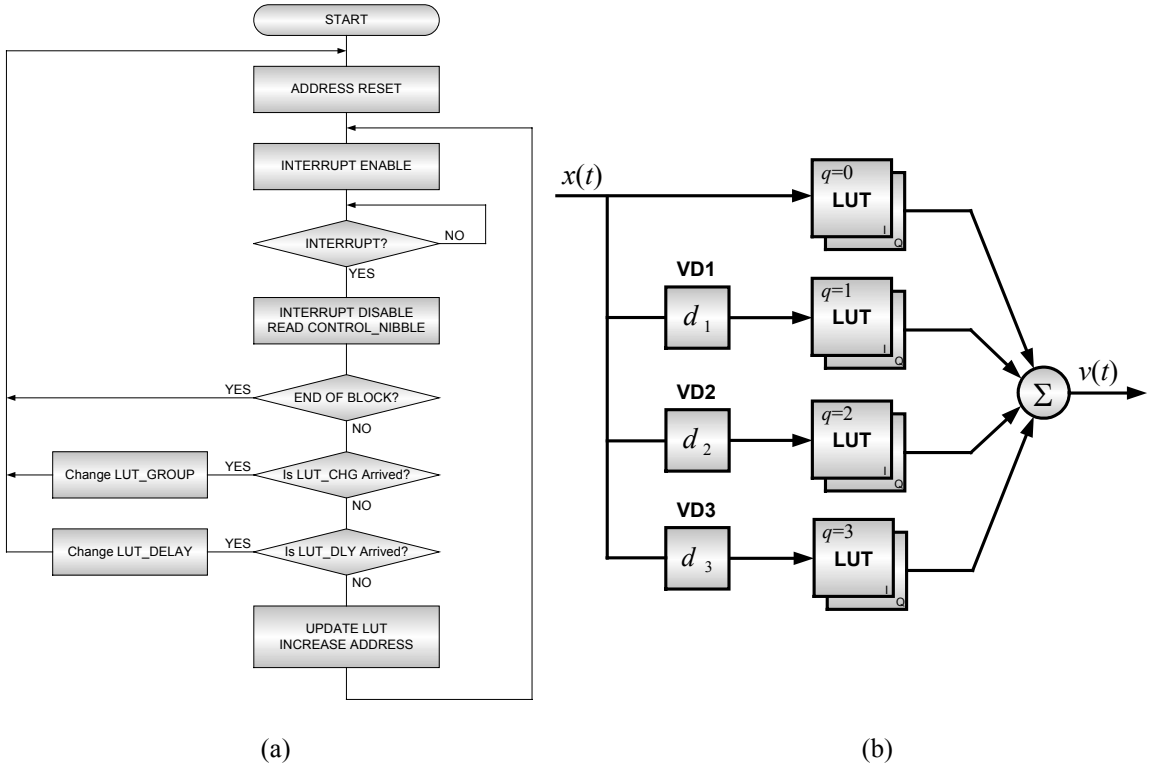
(a)



(b)

Figure 4.4 FPGA LUT design. (a) Functional diagram. (b) Schematic.

An 8-bit embedded microcontroller manages the updating of the LUT contents from the PC through the universal serial bus (USB) connection. Internal and external digital clock managers (DCMs) are used to synchronize all the LUT-relevant components, including the ADC and DAC. To overcome difference in clock speeds between the USB and the FPGA, an asynchronous first-in-first-out (Async FIFO) RAM was inserted between the USB interface and the microcontroller. Figure 4.5 describes a procedure that the embedded microcontroller in the FPGA uses for LUT update.



(a) (b)

Figure 4.5 FPGA LUT update. (a) Flow chart of the embedded microcontroller-based update program. (b) LUT subgroups with a corresponding delay taps.

Whenever a 16-bit data packet shown in Table 4.1 is transferred from a PC, it causes interruption to identify the data. Based on the control nibble (4 most significant bits) of the

packet, the microcontroller changes the delay value of each tap or updates each LUT.

Table 4.1 Bit assignment of a transferred data packet

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control				Data											

Table 4.2 describes the control commands included in the packet that control the operation of the microcontroller.

Table 4.2 Control commands for LUT update

1111b	1010b	1001b	1000b	0100b	0011b	0010b	0001b
End of Block	Delay Tap 3	Delay Tap 2	Delay Tap 1	LUT 3	LUT 2	LUT 1	LUT 0

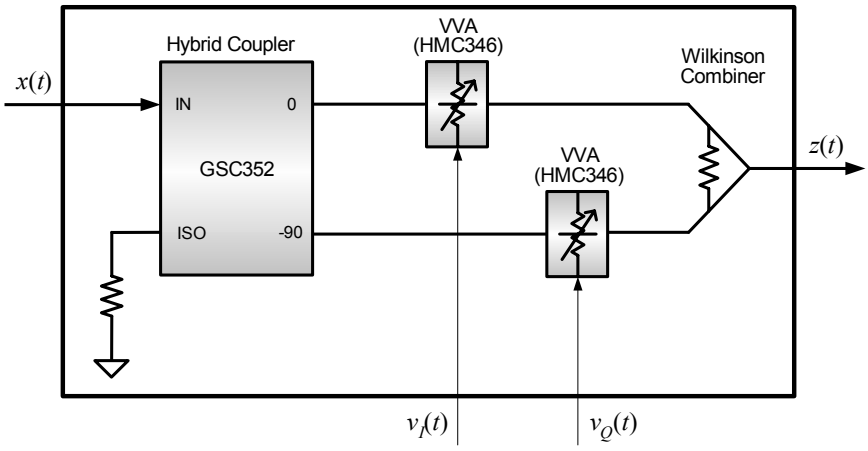
After identifying the meaning of the control nibble, the microcontroller uses the 8-bit control bus to change the address of a LUT, a LUT group, or a variable delay component. Table 4.3 shows the bit assignment of the control bus.

Table 4.3 Bit assignment of the control bus of the microcontroller

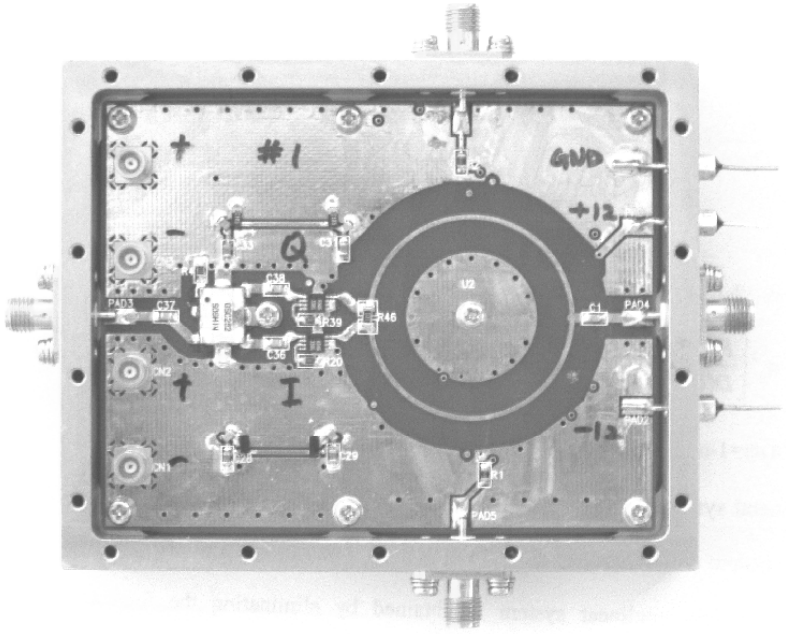
Port 8	Port 7	Port 6	Port 5	Port 4	Port 3	Port 2	Port 1
Variable Delay		LUT Group			Address		Write Enable
01	VD1	100	LUT0		01	Increase	0 Off
10	VD2	101	LUT1		10	Reset	1 On
11	VD3	110	LUT2				
		111	LUT3				

4.4.2 Vector Modulator (VMOD)

The VMOD shown in Figure 4.6 consists of a 90° hybrid coupler, two variable attenuators, and a Wilkinson combiner.



(a)



(b)

Figure 4.6 Vector modulator. (a) Block diagram. (b) PCB assembly.

The RF input is split into I and Q signals by the quadrature hybrid coupler (Soshin GSC352-HYB0900). The variable attenuators (Hittite HMC346MS8G) operate on quadrature signals to produce the desired amplitude and phase values when those signals are summed by the microstrip Wilkinson power divider/combiner. The dynamic area of the VMOD is bound within the fourth quadrant by the 90° hybrid coupler. The VMOD uses variable attenuators that operate on quadrature signals to produce the desired amplitude and phase values when summed. In such a structure, it should be noted that the attenuator control characteristics are not linear. However, the LUT automatically compensates for the errors as it adapts to minimize overall distortion. In addition, the control bandwidth of the attenuator is another important factor for a VMOD because it must process the envelope correction signal without distortion.

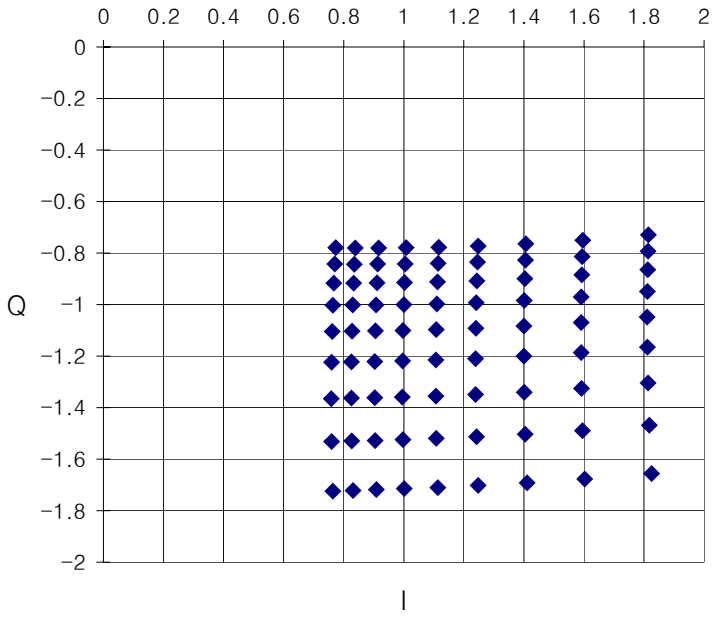
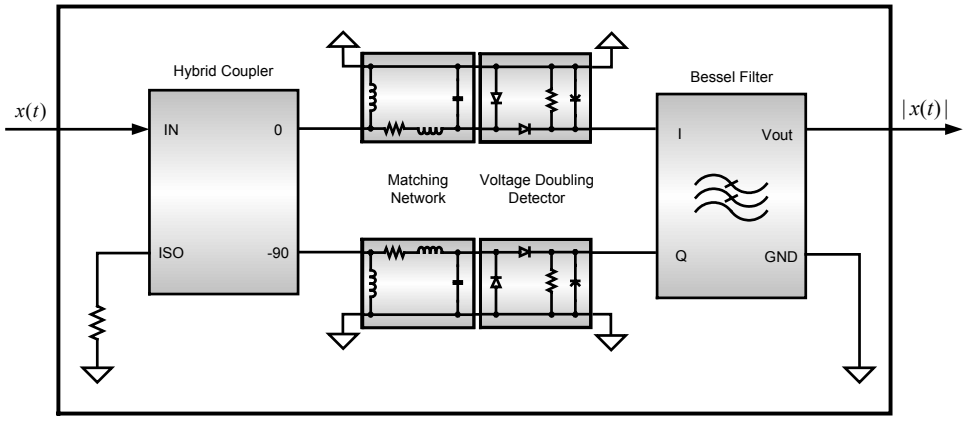


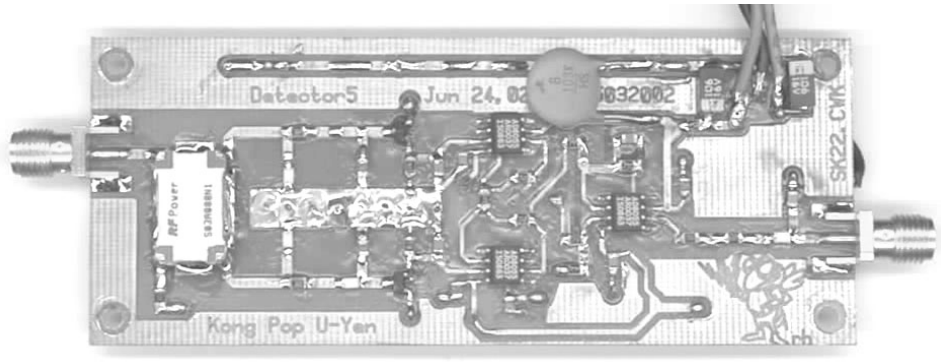
Figure 4.7 Measured VMOD dynamic range.

4.4.3 Envelope Detector (EDET)

Figure 4.8 shows the RF envelope detector that is used for the system to monitor the signal envelope and generate the index values for the LUT. The balanced configuration combined with the matching networks provides a good voltage standing wave ratio (VSWR) and low reverse IMD. The matching network provides the minimum return loss for a signal detector. A 90º hybrid coupler is employed to minimize the reflected odd harmonics. The voltage-doubling detection scheme used in the design gives the voltage level twice as high as that gained with a single diode detector.



(a)



(b)

Figure 4.8 Envelope detector. (a) Block diagram. (b) PCB assembly.

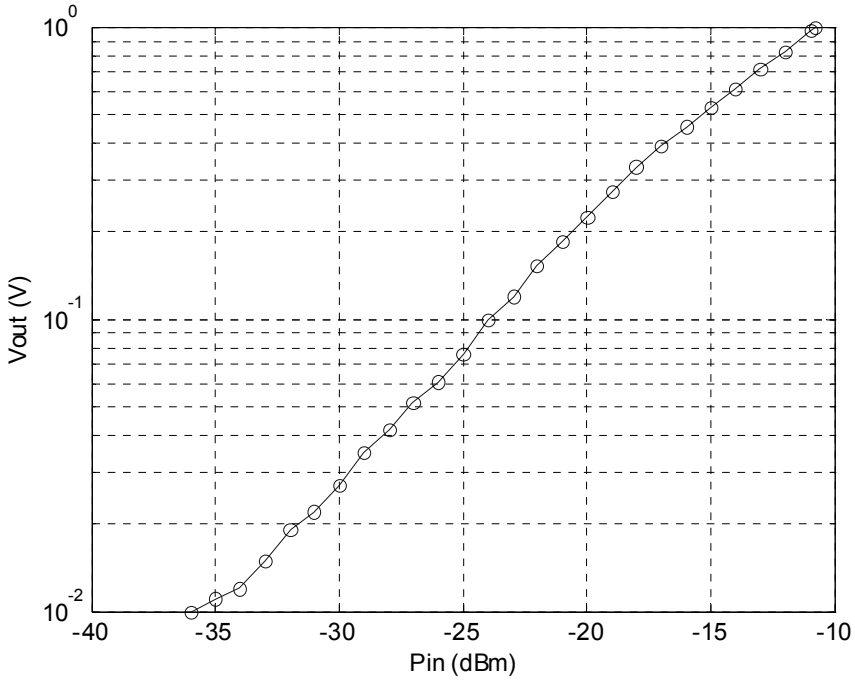


Figure 4.9 Measured output voltage response of the EDET to the input power.

4.4.4 Testbed for the Correction-Loop Subsystem

Figure 4.10 describes the correction-loop subsystem testbed. It extracts predistortion information and validates envelope predistortion performance. The system operates in two stages: (1) calibration and (2) predistortion. In the calibration stage, a VNA is used to obtain nonlinear characteristics inverse to those of the PA and other components along the main RF signal path.

The results from the VNA are used to update the LUT adaptively by using the following *least mean square* algorithm in the PC to minimize the predistortion function error:

$$\mathbf{LUT}_{i+1} = \mathbf{LUT}_i + \mu \cdot \mathbf{e}_i, \tag{4.3}$$

$$\mathbf{e}_i = 1 - \frac{\mathbf{y}_i}{a_1 \cdot \mathbf{x}_i}, \tag{4.4}$$

where $\mathbf{LUT}_i=[lut_i(0), \cdots, lut_i(S\text{-}1)]^T$, S is the LUT size, μ is the convergence factor, $\mathbf{e}_i=[e_i(0), \cdots, e_i(N\text{-}1)]^T$, $\mathbf{x}_i=[x_i(0), \cdots, x_i(N\text{-}1)]^T$, $\mathbf{y}_i=[y_i(0), \cdots, y_i(N\text{-}1)]^T$, a_1 is the linear gain of the PA, i is the number of iterations and N is the number of samples.

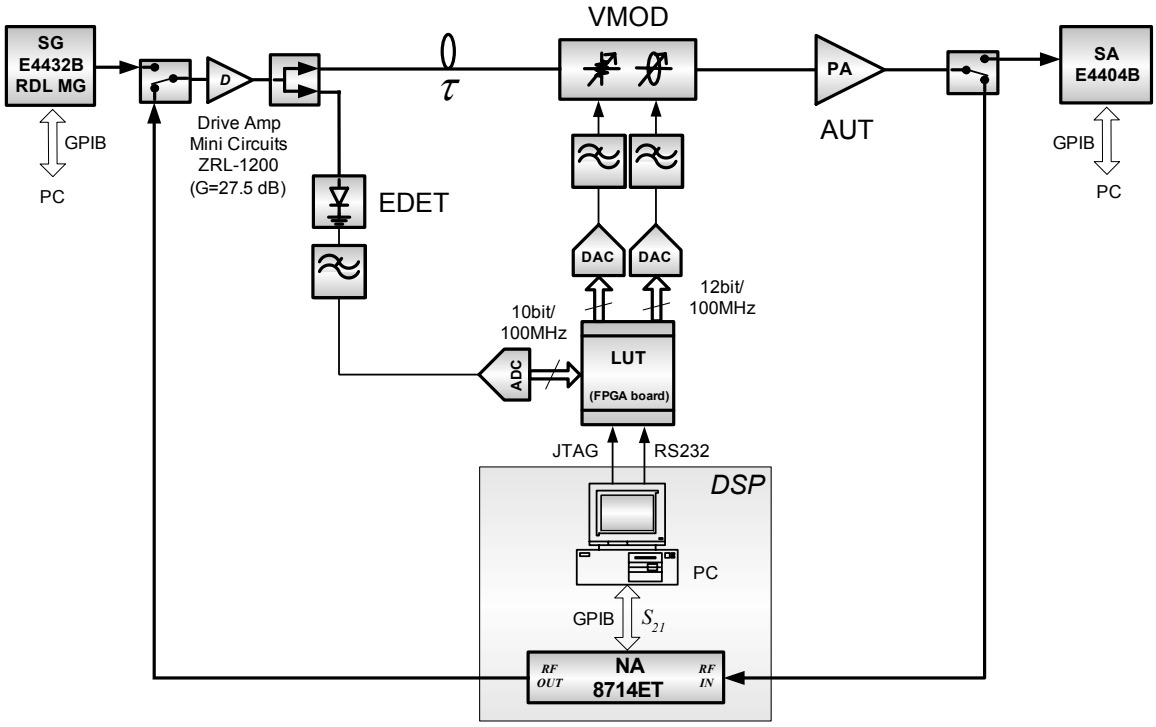
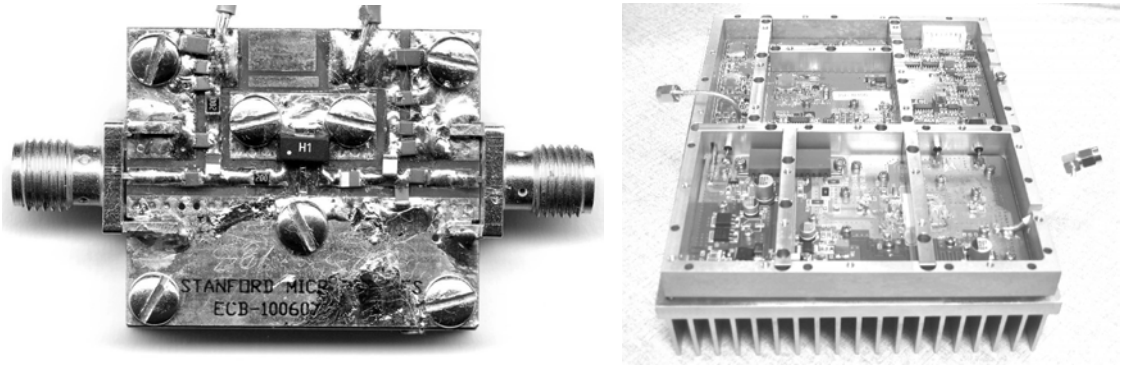


Figure 4.10 Block diagram of the correction-loop test system.

Upon successful calibration of the system, a signal generator is used to generate the signals of interest, and the non-adaptive predistortion performance is measured on the spectrum analyzer in the predistortion stage. An adaptive control may also be required in an actual application to compensate for long-term variations of the amplifier characteristics because of temperature variation, device drift, aging, etc.

4.4.5 Power Amplifiers Tested

Figure 4.11 shows the PAs used to validate the performance of the predistortion system. A low-power amplifier (LPA), the Sirenza SHF-0189, was selected because of its good linearity and low memory effects. The gain was about 16.5 dB, and the output power at 1dB gain compression point (P_{1dB}) was measured as 27 dBm at 881.5 MHz. This single-stage PA was operated in class-AB mode. A higher power amplifier (HPA), which has a peak envelope power (PEP) of 90 W, was also measured to ascertain the limitations that PA memory effects impose on predistortion system. The HPA was composed of three stages in cascade: (a) a 0.13W GaAs MESFET PA (W-J AH1), (b) a 2.5W LDMOS medium power module (Motorola MHL9236), and (c) a 90W PEP LDMOS high PA (Motorola MRF9085). The last two stages are operated in class-AB mode.



(a) (b)

Figure 4.11 Power amplifier used for the wideband correction performance tests. (a) 0.5W PA. (b) 90W PA.

4.4.6 Experimental Results and Analysis

Using 3-carrier cdma2000 and multi-tone signals, the linearization performances for both the 0.5W PA and the 90W PA were examined on the testbed shown in Figure 4.10. Because

the 0.5W PA is a low-power amplifier that shows weak memory effects and a good tolerance for high peak power beyond saturation, it is well suited to validate the performance of the RF envelope predistortion using the LUT correction-loop subsystem and the VNA.

Figure 4.12 shows the before- and after-calibration data of the system with the SHF-0189. The data were obtained by operating the VNA in power sweep mode.

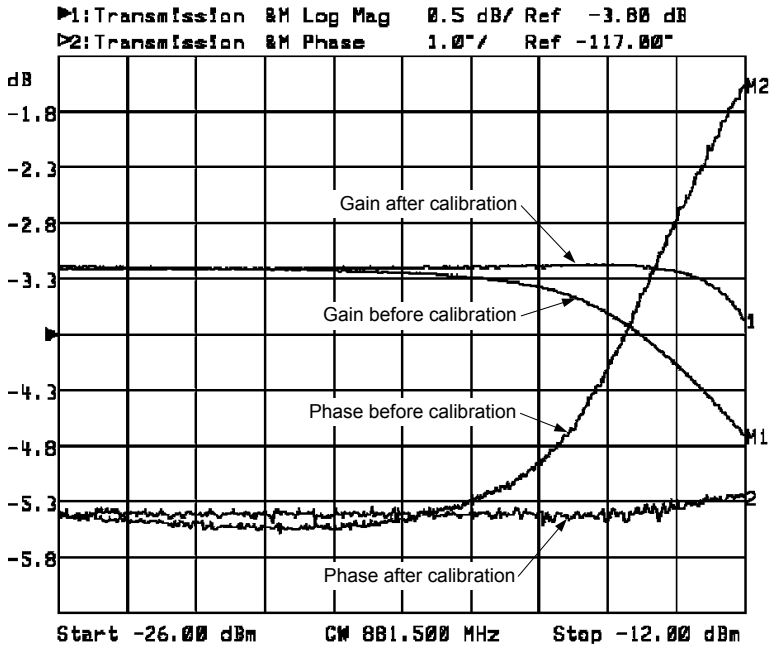


Figure 4.12 System calibration using the VNA.

Predistortion performance depends on the accuracy of this calibration. The experiment demonstrated that up to the clipping level of the PA the gain compression and the phase deviation were corrected to within 0.1 dB and 0.3°, respectively. The steep slope of gain compression shown after calibration indicates the power saturation of the PA. It means that beyond the power saturation level, further predistortion calibration for gain compression

may not be achieved.

Based on the information obtained in the calibration stage, an open-loop predistortion was performed in the predistortion stage. Figure 4.13 shows the spectrum results for the 8-tone signal with a signal bandwidth of 21 MHz. It showed IMD3 suppressions of 9 to 13 dB over 63 MHz. Although a single-tone signal in a power sweep mode was used in the calibration, the wideband 8-tone signal test showed good IMD3 suppression because the LPA has low reactive variation over the frequency range. Because the correction bandwidth heavily depends on the wideband signal handling capability of the correction-loop subsystem, it could further be extended if the sampling rate were increased.

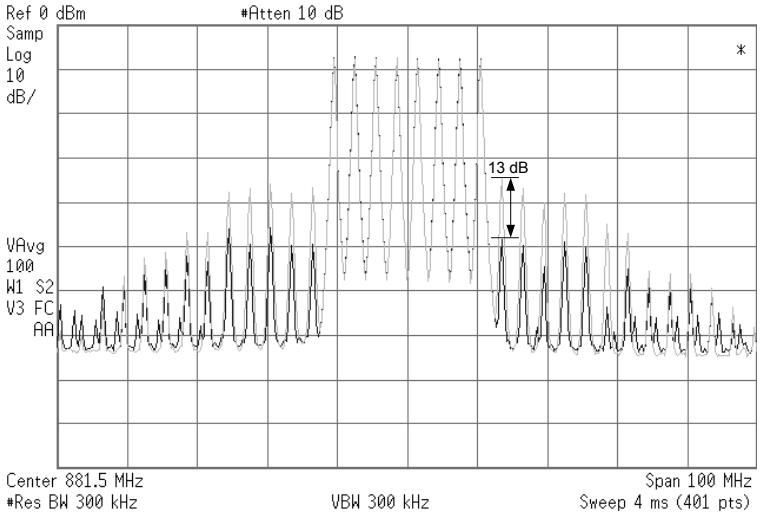


Figure 4.13 8-tone signal test at the 3 MHz of tone spacing (Pout: 20.4 dBm).

Figure 4.14 illustrates the IMD3 ratio improvements over the output power for multi-tone and CDMA signals. This describes the IMD performance with regard to the

relationship of PA nonlinear characteristics and signal envelope statistics. The two-tone signal has statistics that show relatively large amounts of power occurring at high power levels. On the other hand, the 8-tone and CDMA signals have Gaussian distributions that locate most of power around the middle of the dynamic range. The illustration also shows that with the improvements the slopes of the peaks steepen. This occurs because before predistortion the system has more of a compression/deviation property that shows a high order of distortion at the higher power level, but after predistortion it has a linearized property until the occurrence of the peak.

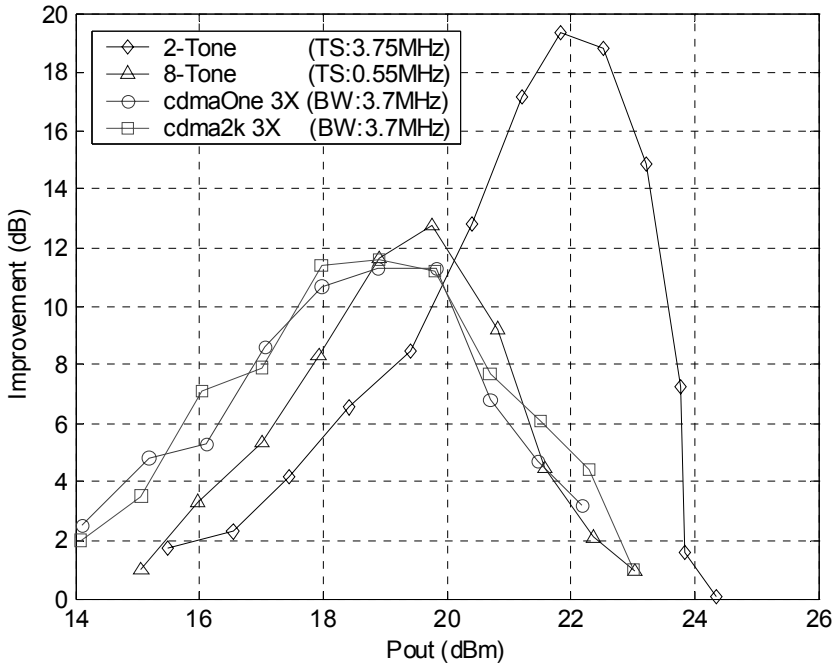


Figure 4.14 IMD and ACPR improvements over the output power: PAPR: 10.5 dB (cdmaOne 3X) and 10.0 dB (cdma2000 3X).

Figure 4.15 is the spectrum results for a 3-carrier cdmaOne signal that has a bandwidth of 3.7 MHz at the center frequency of 881.5 MHz and a PAPR of 10.5 dB. As seen in

Figure 4.15, the system achieved ACPR improvements of 13 dB in the right side and 15 dB in the left side with a 13 dB output power backoff.

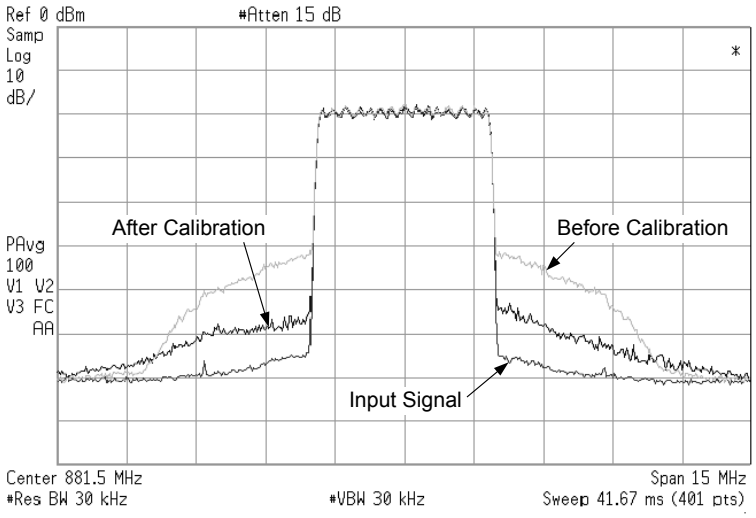


Figure 4.15 cdmaOne 3X signal test for a 90W PEP PA (BW: 3.7 MHz, PAPR: 10.5 dB, Pout: 36.5 dBm).

4.5 SIGNAL INTEGRITY ISSUES

One discovery in the course of developing the system was the importance of the integrity of the high-speed digital signal transmission. Faulty signals caused performance to deteriorate. Various experiments traced this deterioration to crosstalk among high-speed digital buses that adversely affected analog-to-digital conversion. As a result, the ADC was carefully shielded from digital noise and other interference. It was also found that the aperture jitter from the ADC could severely degrade system performance in terms of signal sampling and distortion correction. This led to improvements in the phase noise of the oscillator driving the ADC so that aperture jitter was reduced.

4.5.1 Crosstalk

A sampling rate of 100 MHz was used on the correction-loop subsystem, which is a relatively high-speed signal in terms of the signal integrity issues. When such a high-speed signal is processed, the risk of signal crosstalk and clock signal isolation problem should carefully be considered. Figure 4.16 shows the testbed used to investigate the problem of the integrity of the signal transmitted through the LUT subsystem, which consists of an ADC, an FPGA LUT, and a DAC in series.

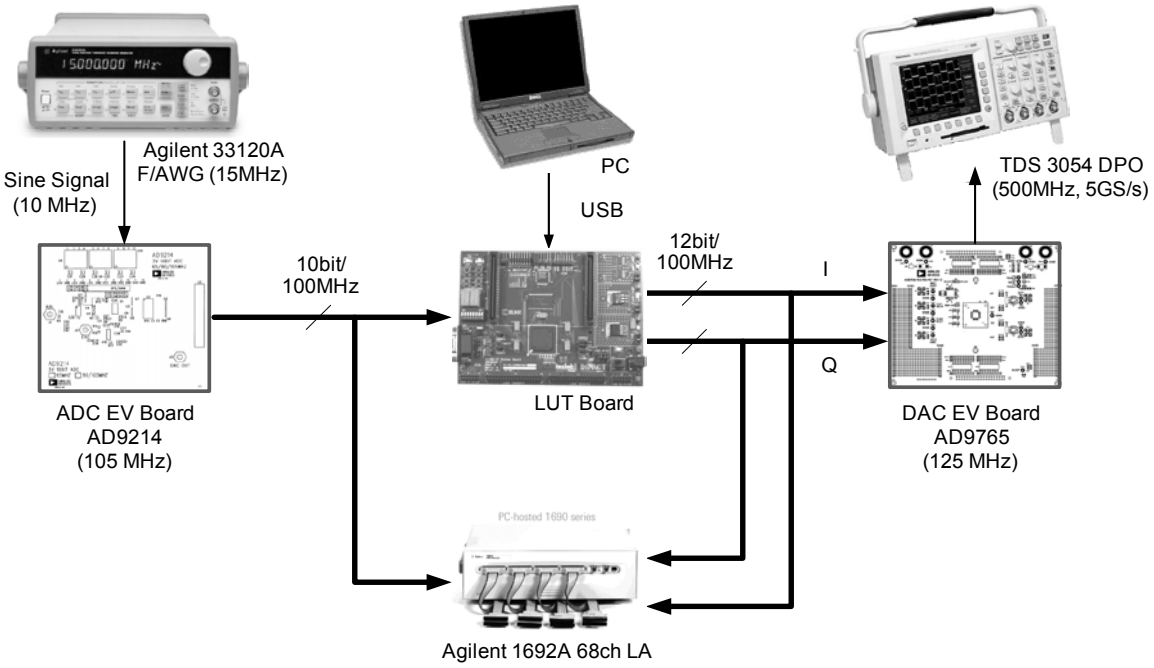


Figure 4.16 Testbed to examine the signal integrity of the LUT subsystem.

The PC forms a linear function in the FPGA LUT through the USB connection. This linear function in the LUT plays a role in replicating the input signal at the output without any distortion or noise so that the integrity of the signal along the path can be examined. A sinusoidal signal with a frequency of 10 MHz was used as the input for the examination.

The analog input signal, which is created by the function generator, is sampled at 100 MHz by the ADC to produce the corresponding 10-bit digital signals that are used as a value to address the LUT. The digitized input signal is then restored from the 12-bit digital signals by the DAC through the LUT. The signals are measured and analyzed with the oscilloscope in the analog domain and the logic analyzer in the digital domain.

4.5.2 Effects of the ADC performance on the subsystem

The performance of the ADC is mainly limited by uncertainty in the sampling process because of aperture jitter over a very wide range of sampling rates. For ADCs operating at a high sampling rate, the speed of the device technology is also a limiting factor because of comparator ambiguity. Comparator ambiguity is caused by unambiguous decisions regarding the relative amplitude of the input voltage. Aperture jitter occurs because an ADC does not sample the input signal at precisely equal time intervals. Also, it can be caused by a sampling clock with a phase noise that generates a sampling uncertainty. When the digital output lines start generating their signals, the signals interfere with each other because of crosstalk. As shown in Figure 4.17, this crosstalk effect on the digital signals may return to the ADC and corrupt the clock signal that determines the sampling time of the input signal. This problem can be reduced significantly by using a twisted-pair ribbon cable. This is because a twisted-pair ribbon cable holds the wires in close physical contact, reducing the separation between the signal and ground. An electrical shield around a digital-bus cable also provides a very low-inductance return path for signal currents and significantly improves signal integrity.

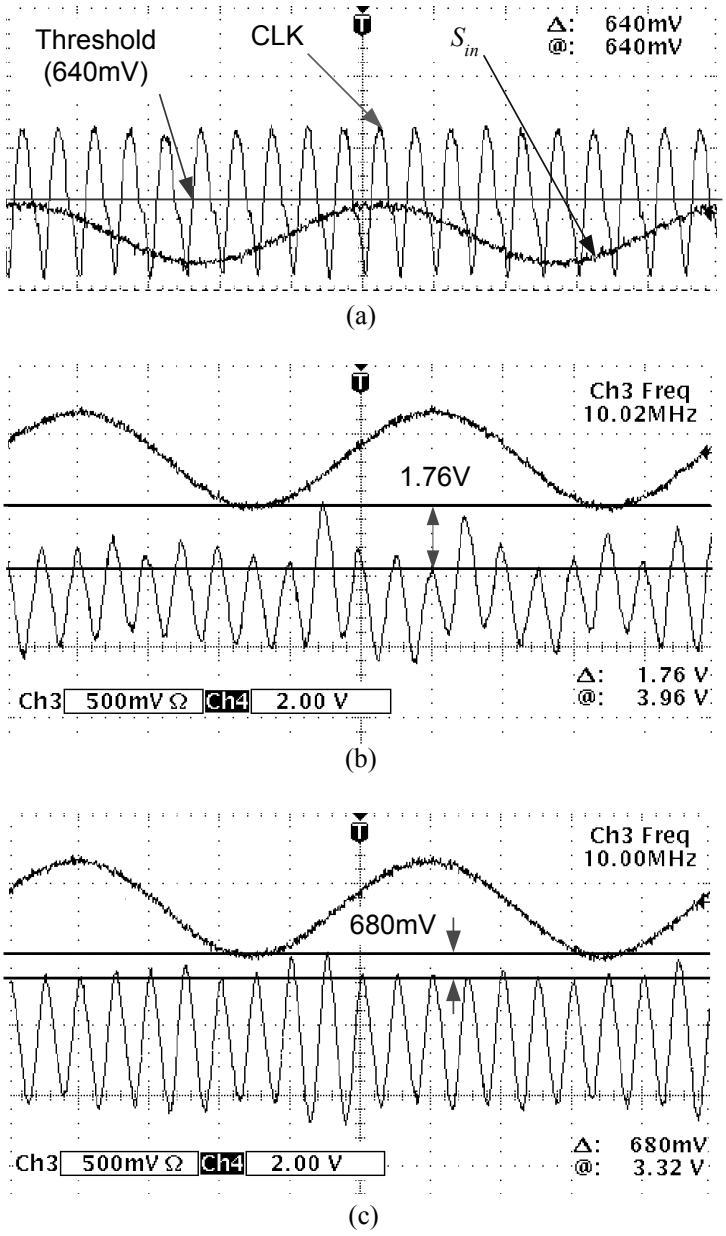
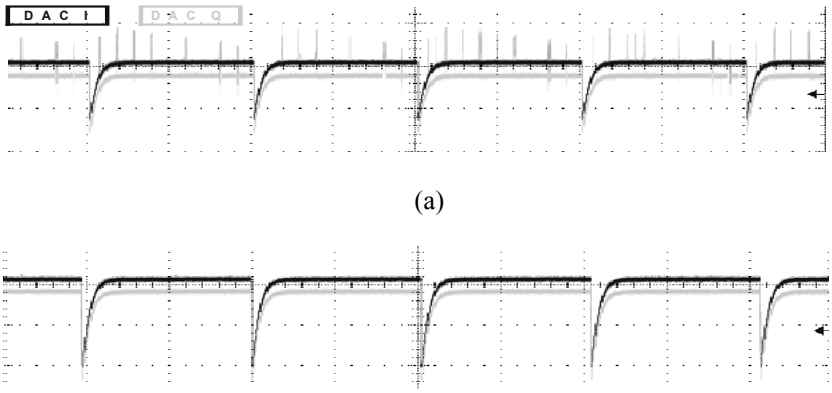


Figure 4.17 Variation of the clock signal integrity depending on the levels of the input signal S_{in}. (a) S_{in} < threshold level (0). (b) $0 < S_{in} < 1024$ with a ribbon cable. (c) $0 < S_{in} < 1024$ with a twisted-pair ribbon cable.

Figure 4.18 and Figure 4.19 show the effect of electrical shielding on noise. The high SNR in the correction-loop subsystem must be maintained to preserve the signal dynamic range on the main RF signal path toward the PA. In Figure 4.18, the differential-shaped

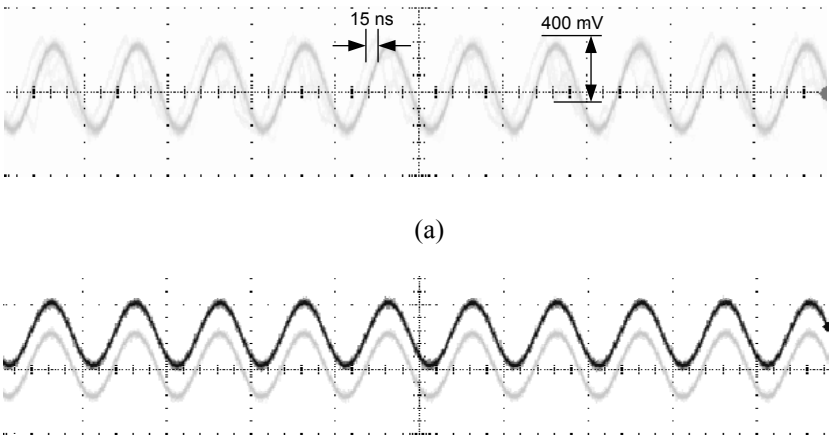
waveform at the output as the response to the burst signal input was created because of a transformer that was used to minimize common-mode distortion. The glitch phenomena at the DAC output, which have an effect on the SNR, was almost removed by the threefold process of isolating the clock signal from the data lines, removing the crosstalk problem on the data lines, and electrically shielding the ADC from noise.



(a)

(b)

Figure 4.18 Output signals of the DAC through the LUT for a 100 kHz burst signal input to the ADC. (a) With ADC unshielded. (b) With ADC shielded.



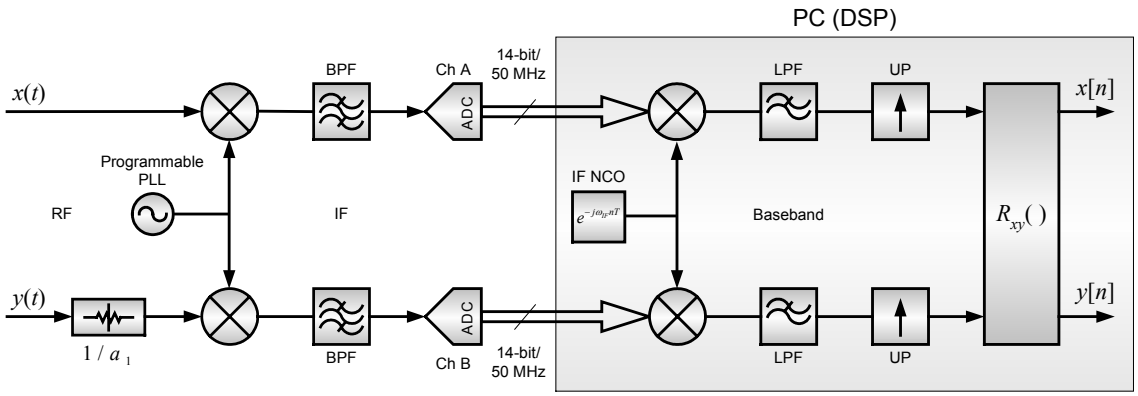
(a)

(b)

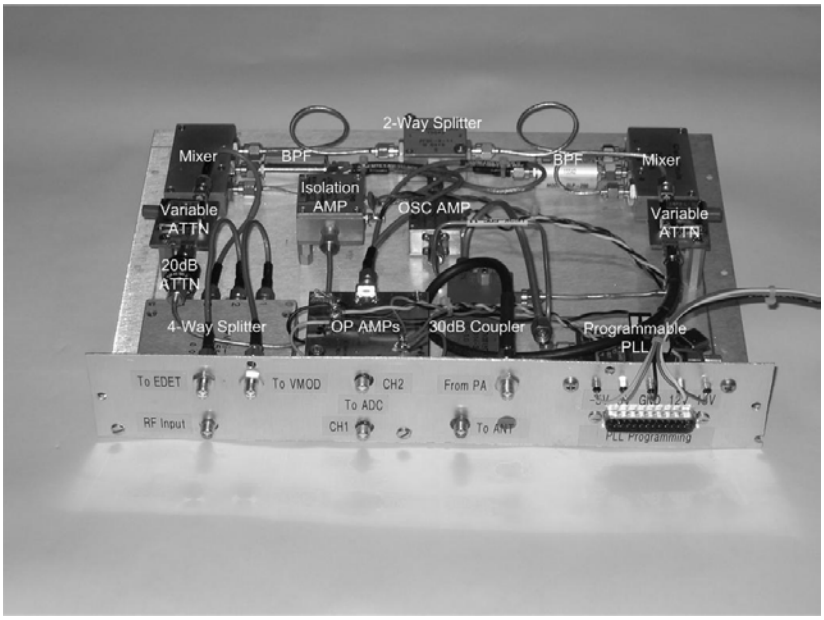
Figure 4.19 Output signals of the DAC through the LUT for a 10 MHz sine signal input to the ADC. (a) With ADC unshielded, DAC I output. (b) With ADC shielded, DAC I and Q outputs.

4.6 CHARACTERIZATION-LOOP SUBSYSTEM

The characterization-loop subsystem for the RF-to-IF downconversion and delay compensation was constructed to characterize the PA nonlinear characteristics, as shown in Figure 4.20.



(a)



(b)

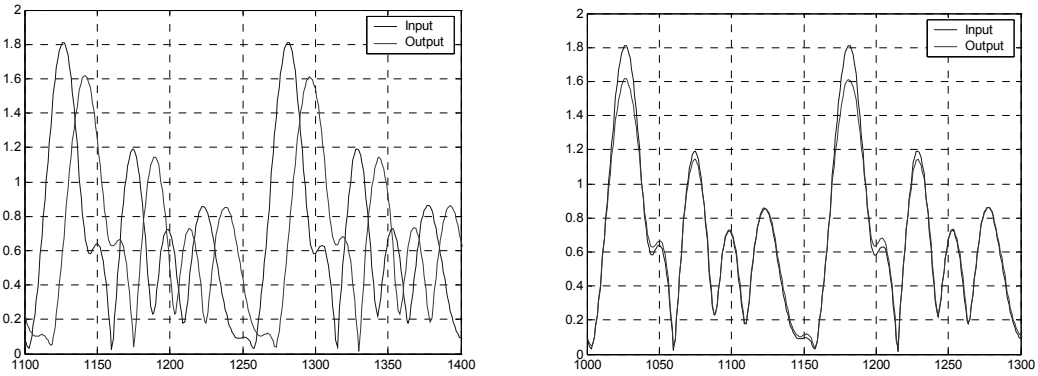
Figure 4.20 PA characterization-loop subsystem. (a) Block diagram. (b) Dual channel RF-to-IF downconverter prototype.

For downconversion, several techniques such as direct downconversion, single downconversion, and double downconversion, can be considered [74]. Since there is no IF stage, the direct conversion scheme (zero-IF frequency) reduces the number of components and the corresponding cost. However, many problems such as oscillation, selectivity, DC offset, etc., are involved in the direct conversion. On the other hand, a technique employing an IF frequency involves a tradeoff between selectivity and sensitivity in terms of signal recovery. The double conversion scheme allows various techniques to improve both selectivity and sensitivity in the IF selection problem, although it requires complex circuitry because of the use of two downconverters. In this system, a single RF-to-IF downconversion scheme was employed to avoid a DC offset problem and complex circuits. The IF signals downconverted from the RF signals are sampled at 50 MHz by a dual channel ADC so that theoretically bandwidth signals up to 25 MHz can be treated. The demodulation to baseband signals is then performed in the digital domain to avoid the IQ mismatch problem.

As shown in Figure 4.21, the delay mismatch between the input and output signals is digitally resolved using a cross correlation method so that no RF delay line is necessary for an extra delay on the reference signal $x(t)$ path. The delay to be corrected, d_x, is determined numerically by locating a point that minimizes the *mean squares error* (MSE).

$$d_x = \min_{0<m<N-W-1} \left\{ \frac{1}{W} \sum_{n=0}^{W-1} \left| x_m[n] - y_0[n] \right|^2 \right\}, \tag{4.5}$$

where x_m and y_0 are the amplitudes of the input and output sequence with the delay m and 0, respectively, W is the window size for comparison, and N is the number of samples.



(a) (b)

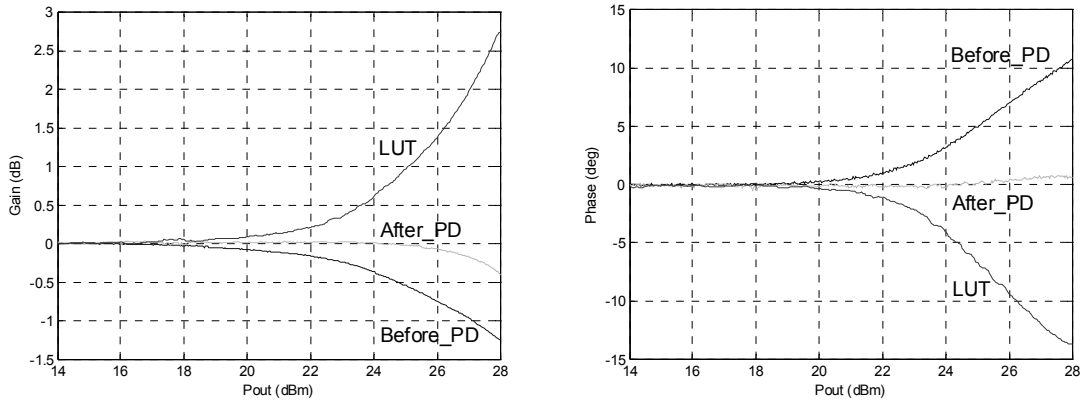
Figure 4.21 Delay compensation in the digital domain. (a) Before compensation. (b) After compensation.

4.7 EXPERIMENTAL VALIDATION OF THE HYBRID EPD SYSTEM

4.7.1 AM/AM and AM/PM Tracking Behavior in LUT

Figure 4.22 shows the predistorting behavior tracked by the LUT to compensate for the gain compression and phase deviation of the 0.5W PA. From Figure 4.22, it is seen that the predistorting function, which was derived by an adaptive estimation of LUT values, required a gain expansion of almost 3 dB and a phase deviation of more than 12° to compensate for the 1 dB gain compression and 8° phase deviation, respectively. These figures are relevant in that they give an estimate of the dynamic range required in the VMOD. As shown in Figure 4.22, because of the nonlinear characteristics stored in the LUT, the resolution of the DAC should be higher than that of the ADC. By using such a structure that includes a LUT, the speed requirements of DSP are greatly reduced because it does not need to operate in real-time. Moreover, it was found that a Nyquist sampling rate of the input signal (as opposed to the wider bandwidth output signal) is adequate to

identify the distortion characteristics of the PA [65].

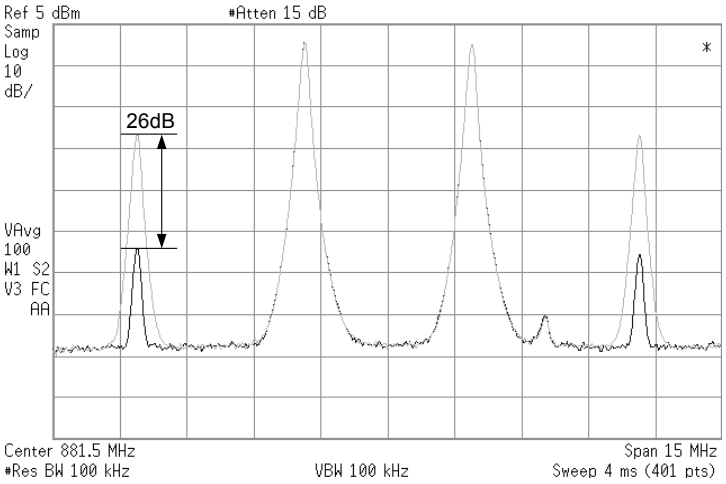


(a) (b)

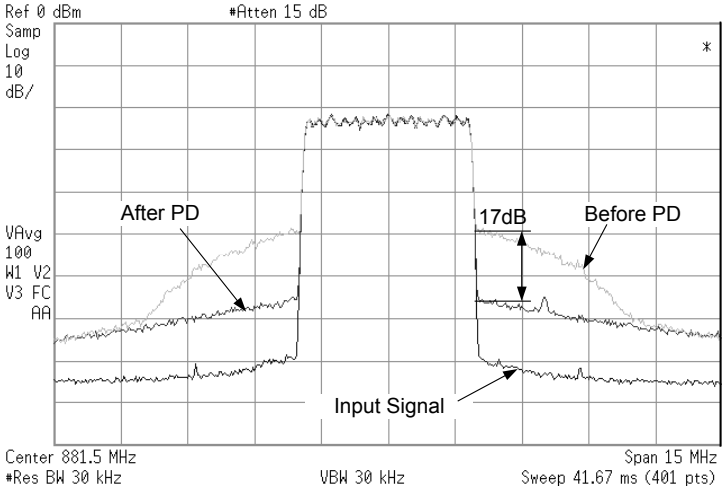
Figure 4.22 AM/AM and AM/PM tracking behavior in LUT. (a) AM/AM. (b) AM/PM.

4.7.2 Narrow Band Signal Test

Figure 4.23 and Figure 4.1 show the predistortion performance spectra that result from the 0.5W LPA and the 90W HPA using a two-tone signal and a cdmaOne 3X signal, respectively. The tone spacing for the two-tone signal test was 3.75 MHz, which was set for comparison with the spread signal with a bandwidth of 3.7 MHz. The ACPR was measured at 2.15 MHz offset from the carrier frequency. For the 0.5W PA, IMD3 for the two-tone test was reduced by 26 dB at an average output power of 20 dBm, while a suppression of 17 dB at an output power of 18 dBm was achieved from the cdmaOne 3X signal.



(a)

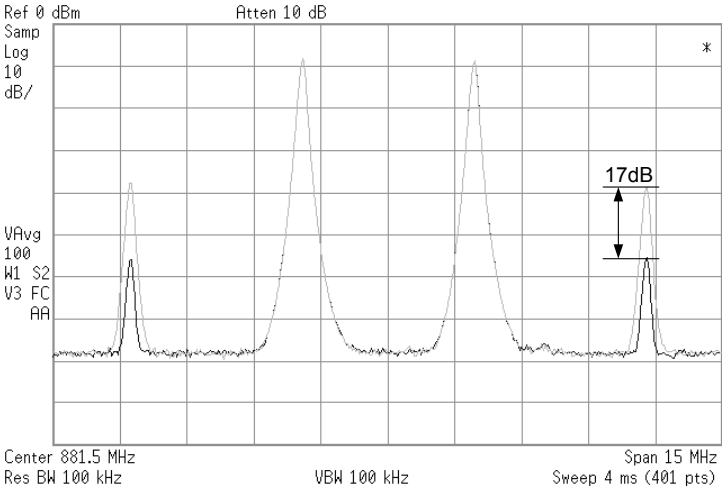


(b)

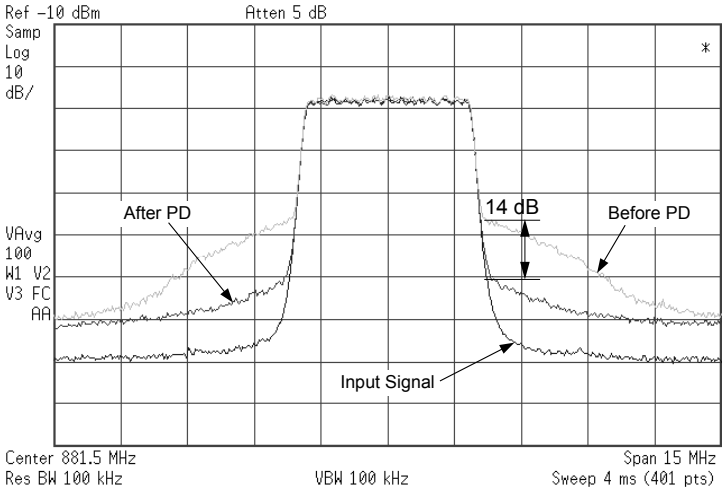
Figure 4.23 Predistortion performance for the 0.5W PA. (a) 2-tone signal test (TS: 3.75 MHz, Pout: 20 dBm). (b) cdmaOne 3X (BW: 3.7 MHz, Pout: 18 dBm).

For the 90W PA, an IMD3 correction of 17 dB was achieved for the two-tone test at an average output power level of 40 dBm, and an ACPR improvement of 14 dB was achieved for the cdmaOne 3X signal test at 39 dBm. As shown in Figure 4.22, it is necessary to drive a relatively large amount of predistorting gain to the input signal to achieve a precise

correction of nonlinearity. However, the necessity of using such a large amount of predistorting gain might exacerbate thermal feedback response. The thermal feedback response can cause a shift in gain or phase as a result of self-heating, and hence also contributes to the envelope frequency response. It results in reduced predistortion performance of HPAs.



(a)

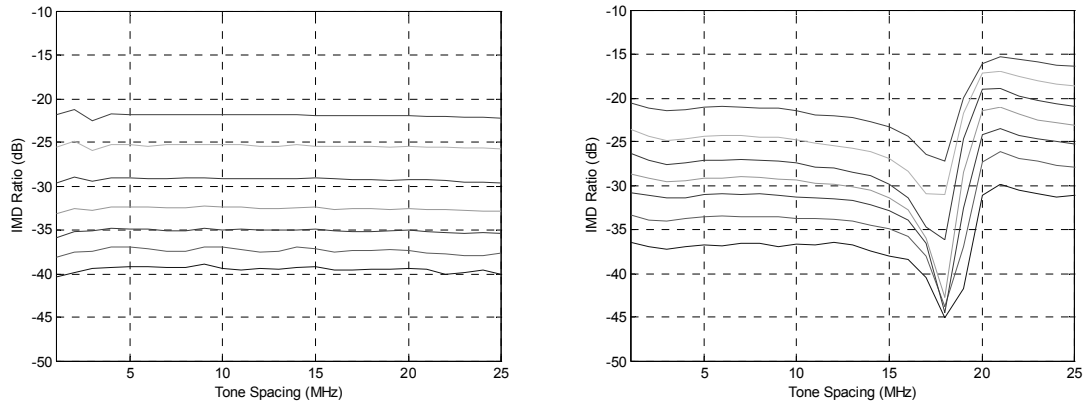


(b)

Predistortion performance for the 90W PA. (a) 2-tone signal test (TS: 3.75 MHz, Pout: 40 dBm). (b) cdmaOne 3x (BW: 3.7 MHz, Pout: 38 dBm).

4.7.3 Wide Band Signal Test

The degree of memory effects for the amplifiers was ascertained by using a two-tone signal with various tone spacings and power levels. As shown by the lack of IMD variations versus tone spacing in Figure 4.24, the LPA exhibits only weak memory effects. In contrast, the IMD varies more than 10 dB for the HPA. It is therefore known to have stronger envelope memory effects [32].

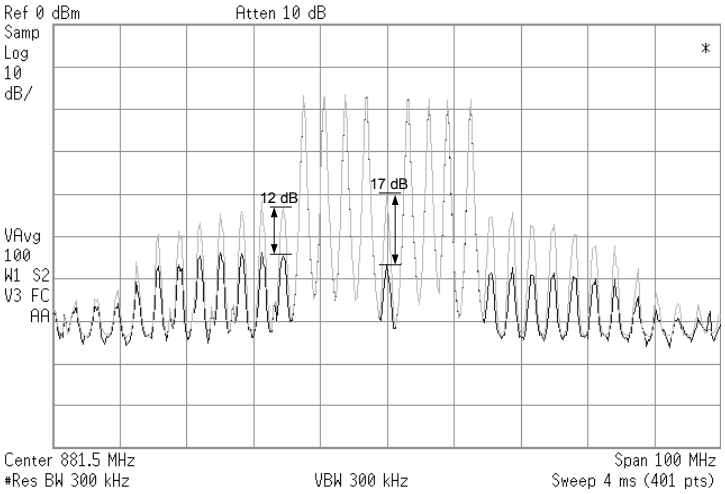


(a) (b)

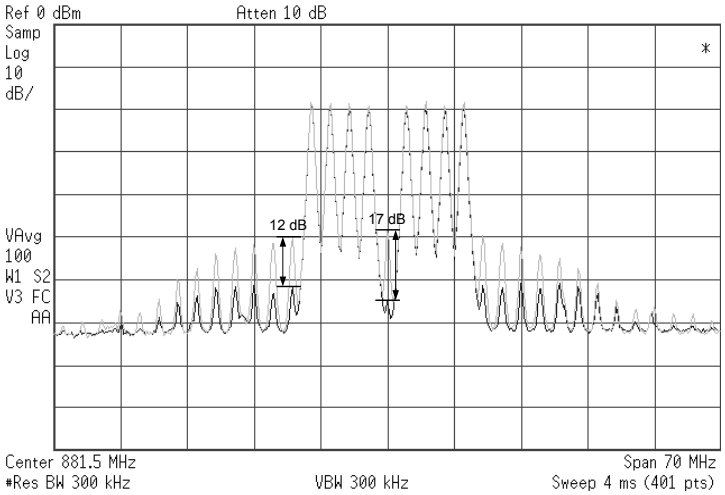
Figure 4.24 Memory measurement results obtained from two-tone tests. (a) 0.5W PA. (b) 90W PA.

Single-tone measurements indicate that the memory effects in the 90W PA are not because of the RF frequency response, but more likely are a result of thermal feedback and bias circuit impedance issues. In theory, compensation for these memory effects could be achieved to some degree by using a more complicated LUT architecture or with a wider bandwidth bias circuit [32], [35]. It was verified for this particular 90W PA that the memoryless predistortion system had limited effectiveness for signal bandwidths exceeding 18 MHz, while the same system exhibited significant predistortion performance

over the maximum tone spacing of 25 MHz for the 0.5W PA, as shown in Figure 4.25. Figure 4.25a shows the spectrum results from the LPA for the eight-tone signal with up to 25 MHz tone spacing.



(a)



(b)

Figure 4.25 Wideband 8-tone signal test. (a) 0.5W PA (BW: 25 MHz, Pout: 21 dBm). (b) 90W PA (BW: 18 MHz, Pout: 39 dBm).

It showed multi-tone IMD suppressions of 12 dB over a 25 MHz BW signal for the 0.5W PA. Wider bandwidths were not attempted because of the limitation in the EDET sampling rate. To examine the in-channel performance, the tones were separated into two groups in which each group has four tones with the middle position empty. Over an 18 MHz BW signal for the 90W PA, the multi-tone IMD was also suppressed by 12 dB, as shown in Figure 4.25b. Suppression performance was about the same as that for the LPA since the magnitude of IMDs because of the memory effects are relatively similar up to 15 MHz. However, as shown in Figure 4.25, beyond 18 MHz BW, the IMD asymmetry notably increases for the 90W PA. If the distribution of signal power over the correction BW allows such envelope memory effects to be excited, significant reductions in the correction capability of the memoryless predistorter can occur.

4.7.4 PA Nonlinearity and Signal Envelope Statistics

Figure 4.26 illustrates a change of PA nonlinear characteristics before and after linearization and statistics of different signal envelopes employed for the experiment. More than 100,000 samples were extracted from each signal to generate the histogram at 10^{-4} probability [2]. The two-tone signal shows a relatively high probability of peak power, but only up to 3 dB above average. On the other hand, the CDMA signal has a Gaussian distribution around the middle of the dynamic range, leading to the high PAPR. IMD suppression is dependent on the signal envelope statistics and the degree of output backoff required to avoid signal clipping.

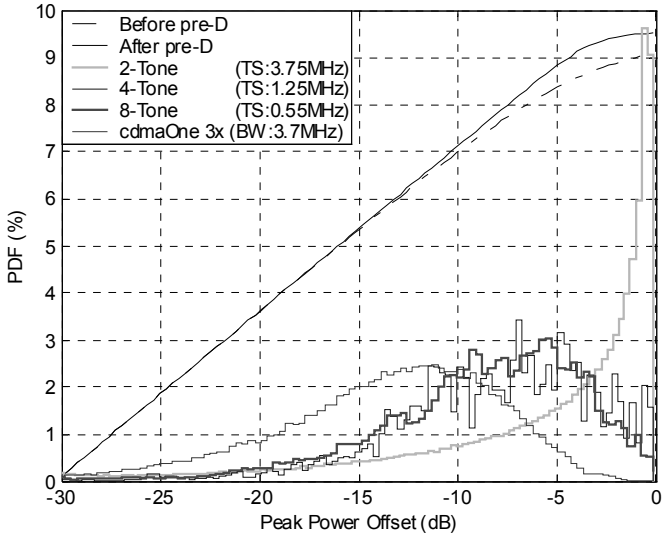


Figure 4.26 PA nonlinearity and signal envelope probability density function (PDF).

The signals have different PAPRs, as shown in Table 4.4. Theoretically, the PAPR of an eight-tone signal would be 9 dB when the eight-tone signal is in a case such that all the tones are in phase. However, there seems to be no chance for all the tones to be exactly in phase during the measuring time period so that the measured result displays only 6.8 dB.

Table 4.4 Peak-to-average ratio for the measured input signals.

Signal	2-Tone	4-Tone	8-Tone	cdmaOne 3x
PAPR (dB)	3	6	6.8	10.5

Note: the 4- and 8-tone signals were a continuous random phase signal.

Figure 4.27 describes IMD3 suppressions over a range of output power for the multi-tone and CDMA signals. It verifies that predistortion performance varies with different signals according to signal envelope statistics, output powers, and PA power capacities. Figure 4.27 shows until peak clipping occurs the suppressions have slopes with dependence on the

signal PAPR over the output power because the PA is operating in the vicinity of the class-A region, and the correction is limited by the system noise floor. At higher operating power, the correction rapidly decreases because of peak envelope clipping effects. In comparison, the results from the HPA have relatively steady IMD suppression performance because the IMD is relatively constant as the result of low idle currents. It means that this HPA operates in more uniform class-AB mode.

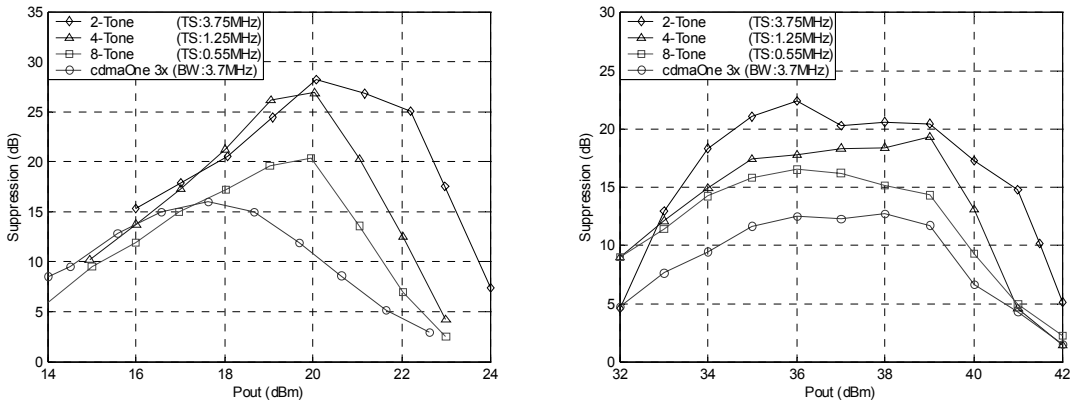
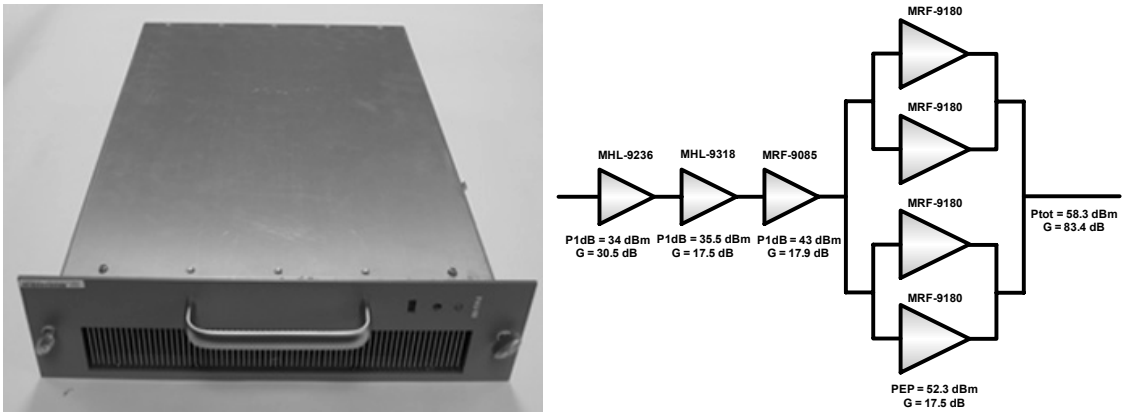


Figure 4.27 Measured predistortion performance vs. output power. (a) 0.5W PA. (b) 90W PA.

4.7.5 Performance Test for a Base Station Amplifier

To validate the performance of this envelope predistortion system for base station applications, a linearization test was performed with a HPA for a cellular-band (869-894 MHz) base station transmitter. Figure 4.29 shows the PA lineup and predistortion performance spectra that result from the 680W PEP HPA using a cdmaOne 3X signal. The PA, which operates in class-AB mode, is composed of four stages in cascade with the final stage in parallel.



(a) (b)

Figure 4.28 Cellular band base station HPA. (a) Danam 680W PEP HPA. (b) PA lineup.

Figure 4.29 shows the spectrum results from the predistortion performance test for a cdmaOne 3X signal. The ACPR was measured at a 2.15 MHz offset from the carrier frequency. An ACPR improvement of 12 dB at 50.5 dBm was achieved for the cdmaOne 3X signal. The asymmetry in the higher order ACPR of the linearized PA indicates that envelope memory effects limit further improvement.

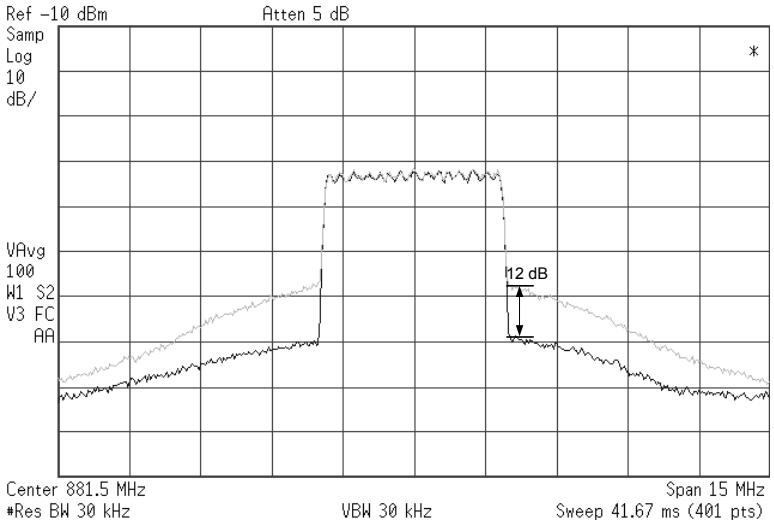


Figure 4.29 cdmaOne 3X signal test (BW: 3.7 MHz, PAPR: 10.5 dB, Pout: 50.5 dBm).

4.8 CONCLUSION

A wideband adaptive predistortion linearization system for PAs with small memory effects was developed based on a high-speed RF envelope modulation that is applied to the input signal of an RF PA. By controlling the vector modulator based on the RF envelope level, the PA is linearized to the extent that memoryless predistortion is possible. The performance of the envelope predistortion system was examined for a 0.5W GaAs HFET, a 90W PEP LDMOS, and a 680W PEP LDMOS PA using multi-tone and CDMA signals. The wideband multi-tone test showed IMD suppressions of 12 dB over a 25 MHz BW signal for the 0.5W PA and the same improvement over an 18 MHz BW for the 90W PA. Over 17 dB and 12 dB corrections for the CDMA signal were achieved for the 0.5W PA and the 90W PA, respectively. The predistortion performance variation for different signals was examined in terms of signal envelope statistics, output power, and PA power capacities. As expected, higher peak-to-average power ratio signals reduce the correction capability of the envelope predistortion system and requires greater output back-off in the PA. In the performance test for the 680W base station HPA, it showed an ACPR improvement of 12 dB for a cdmaOne 3x signal. Further improvement was limited by strong memory effects within the HPA.

It is concluded that RF envelope predistortion linearization provides similar levels of correction as compared with memoryless baseband predistortion, but can achieve wider bandwidths because of relaxed sampling rate requirements.

CHAPTER V

ANALOG ENVELOPE PREDISTORTION

This chapter presents an envelope predistortion linearization architecture that utilizes a direct distortion inverse (DDI) technique and low-power analog components to correct IMD in RF PAs. A gain-phase detector based on log amps is used at the input and output of the PA to estimate the instantaneous complex gain. The outputs of the gain-phase detector are fed back to a voltage-controlled variable attenuator (VVA) and phase shifter (VVP), respectively, to correct any errors in the gain because of AM-AM or AM-PM distortion. As opposed to traditional envelope feedback approaches, this architecture achieves greater bandwidth by only feeding the distortion components (i.e. the deviation from linear gain) back. Moreover, the distortion components are not added to the input signal as feedback, but they are used to predistort the input signal in a multiplicative manner. This architecture also allows correction of envelope memory effects that may occur in the PA. In this chapter, the architecture has been verified by means of computer simulation using behavioral models extracted from a VVA, a VVP, and a 0.5W PA. For a cdmaOne 1X signal, the simulation shows an ACPR peak improvement of more than 10 dB over an output power dynamic range of 6 dB. Based on the simulation results, a prototype of this architecture was implemented. The linearization performances for a 0.5W GaAs HFET and a 90W PEP LDMOS PA were examined.

5.1 INTRODUCTION

Feedback (FB) is commonly known as the simplest and most obvious method of reducing amplifier distortion [1]. However, since RF PAs can have large phase shifts and group delays at gigahertz frequencies, using FB can result in instabilities. To alleviate the drawback of group delay problems in the RF FB, Arthanayake *et al*. proposed an envelope FB technique, which uses a comparison of the source signal and the PA output to extract the PA nonlinear characteristics [9]. If the loop gain is large enough, significant reductions in IMD may be obtained. However, this is gained at the expense of reduced PA gain, and is limited in bandwidth by delays in the envelope signal processing. Jeckeln *et al*. presented a hybrid predistortion approach employing a digital receiver technique to extract PA nonlinear characteristics instantaneously [28]. In this architecture, DSP is applied to the predistorter based on the close comparison of the input and output of the PA. The corresponding DSP-based linearization circuits including signal converters are large and costly, and also use a considerable amount of DC power.

This chapter presents a technique based on an envelope predistortion linearization technique that is used to characterize complex gain in which an analog gain-phase detector are used to provide a simple, efficient and low cost linearization system. Compared with the digital technique, the level of IMD suppression is limited by the accuracy of the analog sub-circuits that subsequently predistort the signal envelope to correct gain errors. The bandwidth is also limited by the delay of the envelope FB loop. However, the simulations using behavioral models extracted from commercially available analog ICs indicate that IMD suppression of more than 20 dB may be achieved over bandwidths exceeding 1 MHz.

Also, the results obtained from prototype experiments verifies the performance of the architecture for CDMA applications.

5.2 ENVELOPE PREDISTORTION USING DIRECT DISTORTION INVERSE

As shown in Figure 5.1a, conventional architectures using an envelope feedback technique use $x(t)$ as the reference signal to calculate the predistortion function $F\{\cdot\}$. The outputs of the linearizer drive a vector modulator to counteract any gain errors. In this manner, $F\{\cdot\}$ is the polynomial pre-inverse of $G\{\cdot\}$. The output of the PA, $y(t)$, can be described as

$$\begin{aligned} y(t) &= z(t)\cdot G\{|z(t)|\} \\ &= \left[x(t)\cdot F\{|x(t)|\}\right]\cdot G\{|x(t)\cdot F\{|x(t)|\}|\}, \end{aligned} \tag{5.1}$$

where the gain function may be estimated by

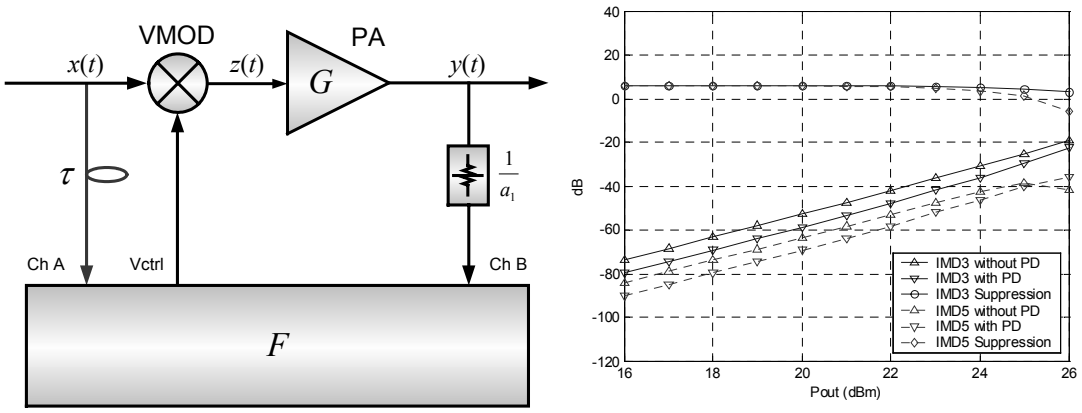
$$G\{|x(t)\cdot F\{|x(t)|\}|\} \cong \sum_{k=1}^{n} a_k \cdot |x(t)\cdot F\{|x(t)|\}|^{k-1}, \tag{5.2}$$

and

$$F\{|x(t)|\} = Polynomial\ \ pre-inverse\ of\ G\{|x(t)\cdot F\{|x(t)|\}|\}, \tag{5.3}$$

where $x(t)$ is the input signal, $z(t)$ is the predistorted input signal to the PA, $G\{\cdot\}$ is the complex gain function of the PA, $F\{\cdot\}$ is the predistortion function, and a_k is the complex coefficient of kth order. In this case, the non-ideality of vector modulation is included in predistortion function calculation and can be corrected. However, the calculation of a correct predistortion function, which is the reciprocal of $G\{\cdot\}$, is complicated. While the predistortion function may be identified by DSP algorithms using a digital look-up table, its implementation in analog form is not straightforward. Consequently, this architecture

cannot perform well in an analog-circuit implementation. Figure 5.1b shows simulation results obtained by using the predistortion function that is calculated from comparison of $x(t)$ and $y(t)$. The simulation results show only 6-7 dB correction.



(a) (b)

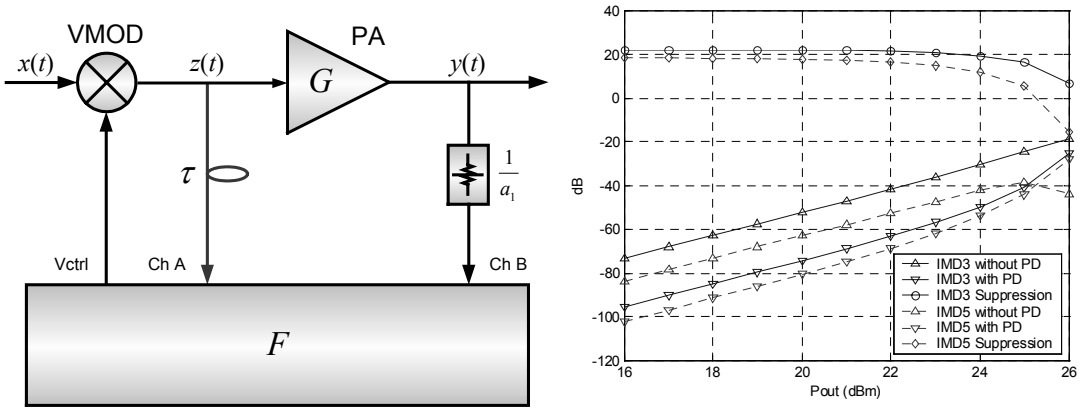
Figure 5.1 Conventional predistortion technique using envelope feedback. (a) Architecture. (b) Simulation results (signal: 2-tone).

In contrast, the DDI-based architecture shown in Figure 5.2a uses $z(t)$ as the reference signal so that the function $F\{\cdot\}$ is simply the reciprocal of the function $G\{\cdot\}$. In this case, the calculation of a predistortion function $F\{\cdot\}$ is straightforward and may be done by analog components. The output of the PA, $y(t)$, can be described as

$$\begin{aligned} y(t) &= z(t)\cdot G\{|z(t)|\} \\ &= \left[x(t)\cdot F\{|z(t)|\}\right]\cdot G\{|z(t)|\}, \end{aligned} \tag{5.4}$$

$$F\{|z(t)|\} = a_1 \cdot G^{-1}\{|z(t)|\}, \tag{5.5}$$

where a_1 sets the overall linear gain of the system. Figure 5.2b shows improved suppression performance compared with that of conventional architectures. The time delay τ is used mostly to equalize the delay between $z(t)$ and $y(t)$.



(a) (b)

Figure 5.2 Envelope predistortion technique using the DDI. (a) Architecture. (b) Simulation results.

5.3 ANALOG ENVELOPE PREDISTORTION SYSTEM

This section describes the detail of an analog EPD linearization system, which is based on the DDI and uses low-power analog components to correct intermodulation distortion in RF PAs. The reciprocal complex gain function of a PA is calculated by the gain and phase detection block. Then, the information from the detection block is used to predistort the input signal in a multiplicative manner so that any errors in the gain because of AM-AM or AM-PM distortion can be corrected. By using a closed loop instantaneous correction, this architecture provides an intrinsic capability to compensate within loop bandwidth for a PA memory effect. As previously mentioned, compensation for a group delay in a PA may be achieved by using a transmission line.

Figure 5.3 illustrates the details of the envelope predistortion linearization architecture using the DDI technique.

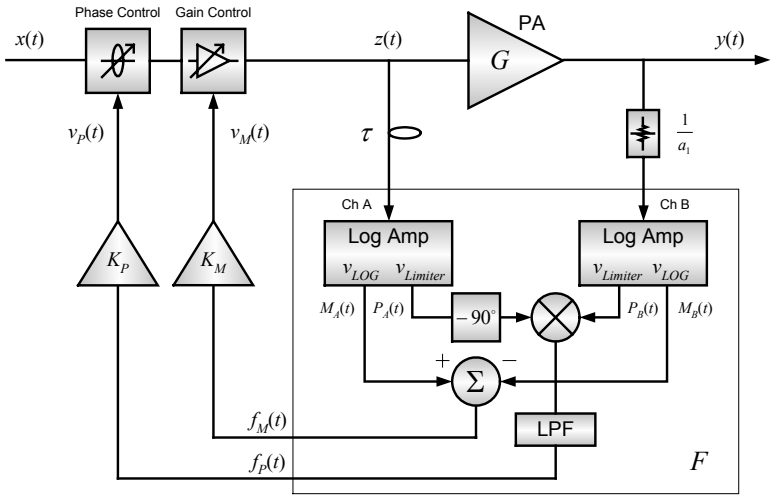


Figure 5.3 Envelope predistortion linearization using the direct distortion inverse technique.

The reciprocal gain function in the predistortion function $F\{\cdot\}$ may be implemented with a commercially available log amps by subtracting the two outputs, as described in [76]. Likewise, phase detection may be implemented by multiplying the limited outputs from the log amps. In this fashion, the VVA control signal $v_M(t)$ and VVP control signal $v_P(t)$ are generated as

$$v_M(t) = K_M \cdot \log \frac{M_A(t)}{M_B(t)}, \tag{5.6}$$

$$v_P(t) = K_P \cdot \left\{ \angle P_A - \angle P_B - 90^\circ \right\}, \tag{5.7}$$

where $M(t)$ and $P(t)$ are the logarithmic and limited output to the input waveform, respectively. Also, K_M and K_P are the scaling factor for magnitude and phase, respectively. While the VVP must be linear in terms of degree/V, a linear dynamic range of 20° may be achievable easily by a reflection-type phase shifter [77].

In addition to the errors induced by the analog components, the correction is also affected by delays around the correction loop. While the compensation for the PA group

delay may be achieved by using a delay line as shown in Figure 5.3, similar compensation for the delays within the envelope predistortion loop cannot be accomplished. This is the primary limitation on the correction bandwidth obtainable by this method. It should be noted that the architecture described in this chapter could correct envelope memory effects within the loop bandwidth. It cannot, however, correct memory effects related to RF frequency response or high-frequency bias effects. Like feed-forward linearization schemes, this architecture requires that the PA have magnitude and phase responses that are as flat as possible over the correction bandwidth. Limitations induced by this effect were discussed in [34].

5.4 SIMULATION MODELS

Figure 5.4 illustrates the schematic for the system simulation of the analog EPD. The behavioral models for simulation were constructed based on the measured transfer characteristics or on the data of datasheets.

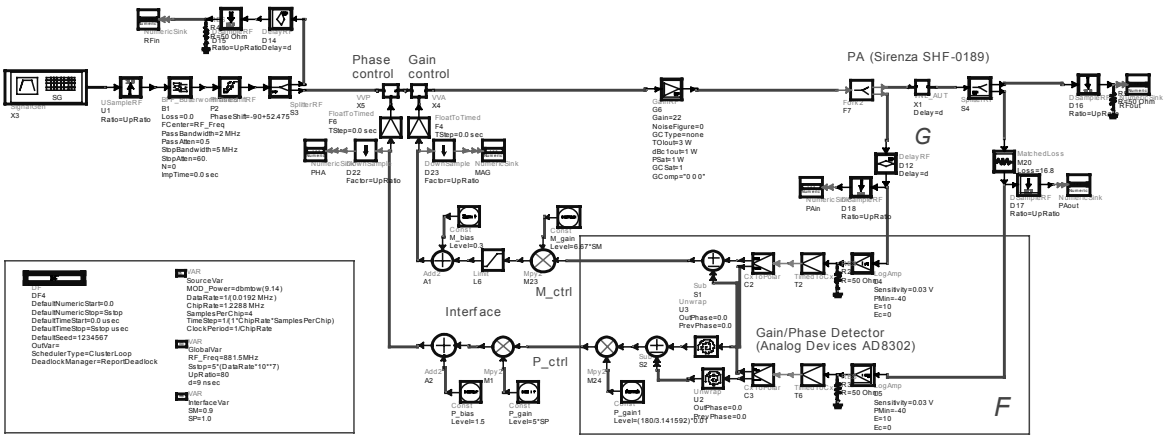


Figure 5.4 Schematic for the ADS system simulation.

5.4.1 Class-AB Power Amplifier Model

In this section, a behavioral model for the class-AB PA was developed for gain y_A and phase y_Φ to fit the measured data, based on the Rapp model [76].

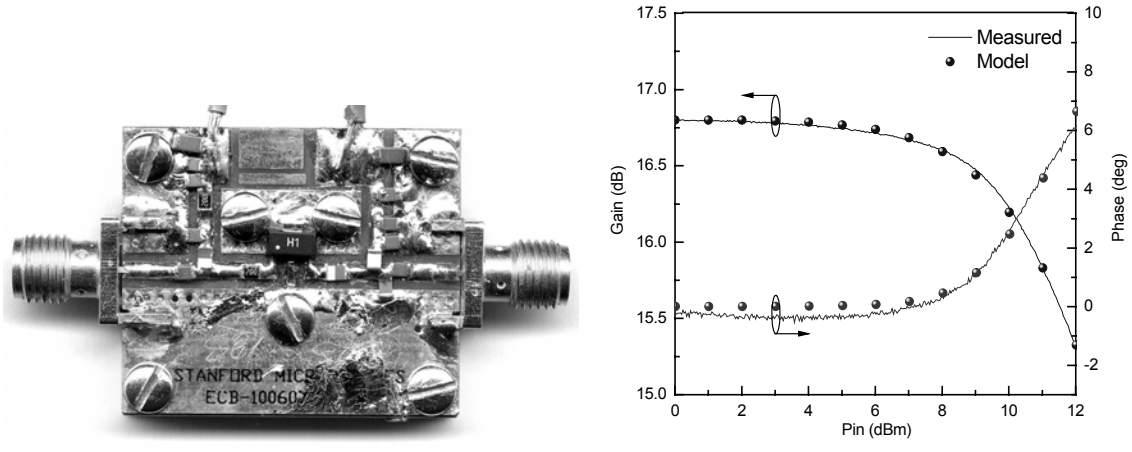
$$y_g = O_g \cdot \frac{L_g}{\sqrt[S_g]{1+\left(L_g / |x|\right)^{S_g}}}, \tag{5.8}$$

where O_g, L_g, and S_g are the offset, the limit, and the smoothness for gain, respectively. Also, $|x|$ is the input amplitude.

$$y_\Phi = 10\log_{10}\left[O_p \cdot \left\{ \frac{|x| \cdot \sqrt[S_p]{1+\left(L_p / |x|\right)^{S_p}}}{L_p} \right\}^{E_p} \right], \tag{5.9}$$

where O_p, L_p, S_p, and E_p are the offset, the limit, the smoothness, and the expansion factor for phase, respectively.

The behavioral model for the amplifier tested, which is shown in Figure 5.5, was extracted from a 0.5W GaAs HFET PA (Sirenza SHF-0189) at 881.5 MHz by fitting the measured AM-AM and AM-PM distortion.



(a) (b)

Figure 5.5 0.5W PA. (a) PCB. (b) Nonlinear transfer characteristics.

Table 5.1 shows the parameter values of the complex gain extracted from the 0.5W PA using (5.8) and (5.9).

Table 5.1 PA model parameters

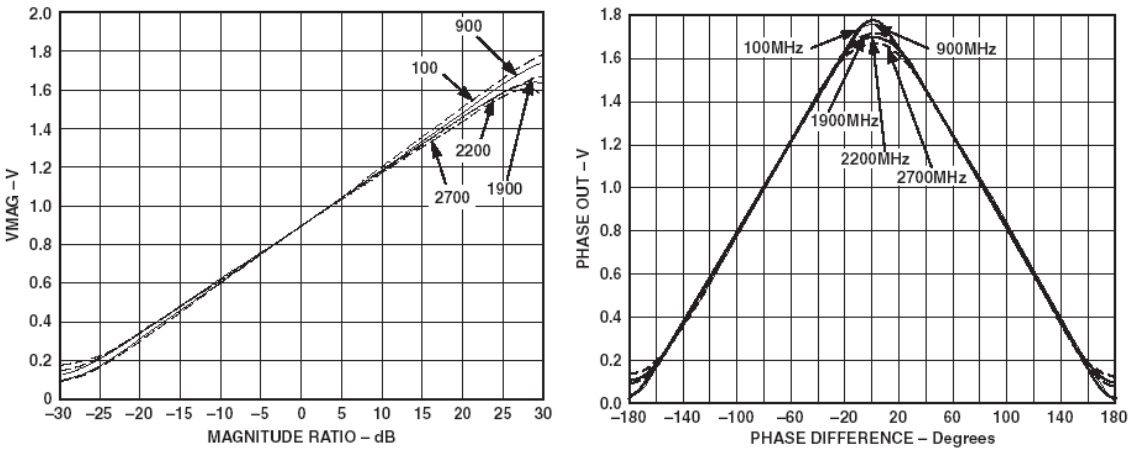
Gain Parameter	O_g	L_g	S_g	
Value	*dBToV(16.8)	**dBmToV(28.2-16.8)	5.25	
Phase Parameter	O_p	L_p	S_p	E_p
Value	*dBToV(0)	**dBmToV(10.4)	9.5	5.0

*dBToV(·)is the scaling function that converts a decibel-scaled input to a linear-scaled output.
**dBmToV(·) is the scaling function that converts a decibel-to-millwatt-scaled input to a linear-scaled output.

5.4.2 Gain and Phase Detection Using Logarithmic Amplifiers

Log amps provide a logarithmic compression function that converts a large range of linear-scaled input signal levels to a decibel-scaled output. Using the difference in the output of two identical log amps and the multiplication of the hard-limited outputs of each log amp, detection of the gain and phase of nonlinear devices can be done easily, as illustrated in Section 5.3. Recently, a gain-phase detector has become commercially available to process the high frequency signals and deliver the gain and phase information of PA nonlinear characteristics instantaneously [76]. Because a large linear dynamic range of more than ± 20 dB and ± 30° is available through the gain-phase detector, an accurate measurement of the instantaneous PA complex gain is possible. However, the gain-phase detector has difficulty measuring zero-crossing signals such as those that are QPSK-modulated because of detection uncertainty created by noise at low levels. In the simulation, the detector model was constructed based on the measurement data in the

datasheet of Analog Device's AD8302 gain-phase detector [79]. Figure 5.6 shows the detector response modeled in the simulation.



(a) (b)

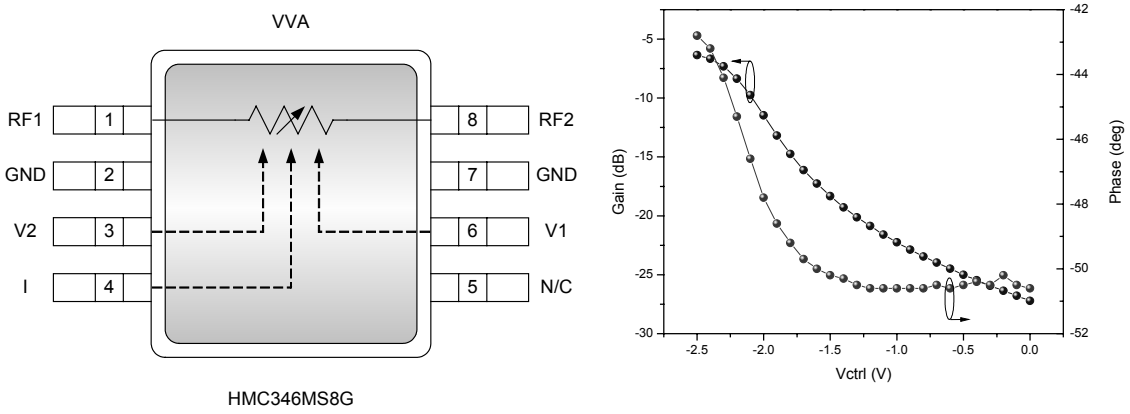
Figure 5.6 Responses of the gain-phase detector (AD8302) [79]. (a) Gain. (b) Phase.

5.4.3 VVA and VVP for the Vector Modulation

Ideal VVA and VVP would have zero phase shift and gain variations as well as linear gain and phase response, respectively. Because the predistortion architecture using the DDI technique does not include the VVA and VVP in the characterization loop and cannot correct their non-idealities, it should be noted that the non-idealities in both VVA and VVP might contribute to limitations in predistortion correction.

Figure 5.7 shows the VVA. Because most VVAs have a log-linear characteristic (dB/V), the logarithmic magnitude output from the gain-phase detector can provide the correct control signal precisely to predistort the envelope of the input RF signal. A commercially available VVA (Hittite HMC346MS8G) shown in Figure 5.7a was used for the gain control. Figure 5.7b shows the measured characteristics of the VVA as a function of

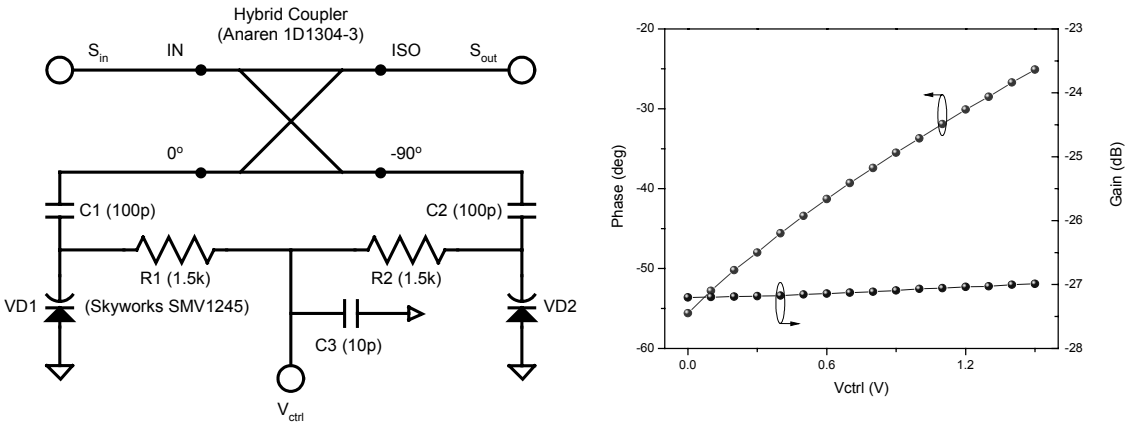
control voltage and indicates a large phase deviation. However, the large phase deviation in the VVA may be improved or removed by using a PIN diode reflection-type variable attenuator [80]. According to Figure 5.7b, a dynamic range from –1.5 voltage to 0 voltage is acceptable so that the linear gain control of 7-8 dB are available.



(a) (b)

Figure 5.7 VVA. (a) Schematic. (b) Measured responses over the control voltage at 881.5 MHz.

In contrast to the VVA, a customized reflection-type VVP shown in Figure 5.8a was implemented for phase control. Reflection-type phase shifters have been widely used to achieve constant phase over a wide frequency range [81]. Figure 5.8b indicates that the gain variation of this VVP is negligible over the control range. Previous measurements with regard to phase correction indicated that the linear dynamic range of 15-20° phase shift was enough to correct the phase deviation of PAs [72].



(a) (b)

Figure 5.8 VVP. (a) Schematic. (b) Measured responses over the control voltage at 881.5 MHz.

Using a least squares fitting method, the polynomial coefficients for the modeling of the VVA and VVP were extracted from the measured data, as shown in Table 5.2.

Table 5.2 Polynomial coefficients of the VVA and the VVP model

		C_0	C_1	C_2	C_3	C_4	C_5
VVA	Gain	-23.26	3.91	1.40	-1.48	1.27	-0.22
	Phase	-49.81	0.60	-3.29	3.57	-1.71	0.32
VVP	Gain	-1.59	-0.08	-0.04	0.11	-0.08	0.02
	Phase	-83.58	33.41	-21.64	22.52	-13.63	3.22

5.5 SIMULATION RESULTS AND DISCUSSION

Using two-tone and cdmaOne signals, the architecture illustrated in Figure 5.3 was simulated in an Agilent ADS™. In the predistortion performance simulations, a FB delay of 9 ns was assumed, including the PA delay of 1.4 ns shown in Figure 5.9 and the delay of other circuits on the DDI loop.

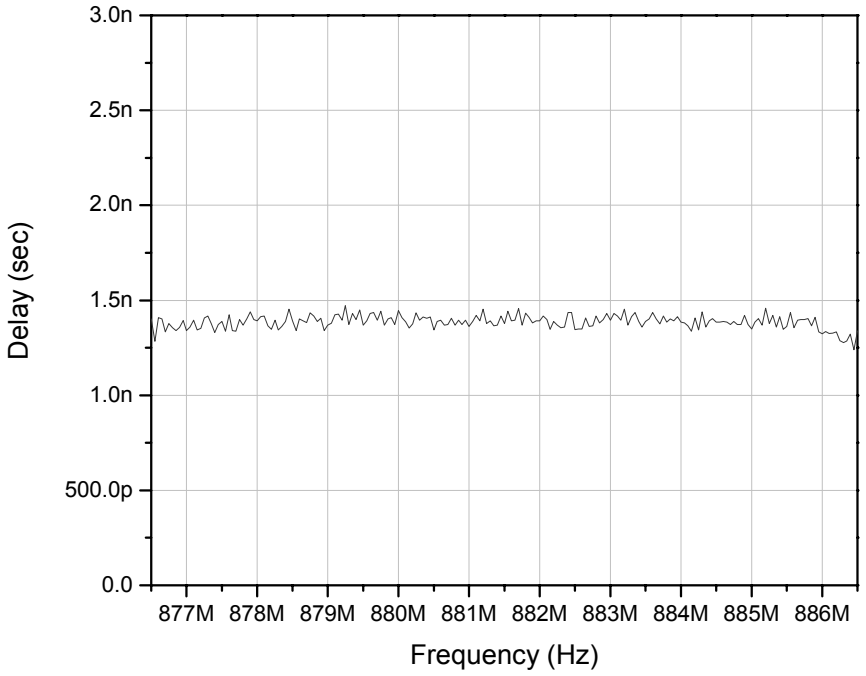
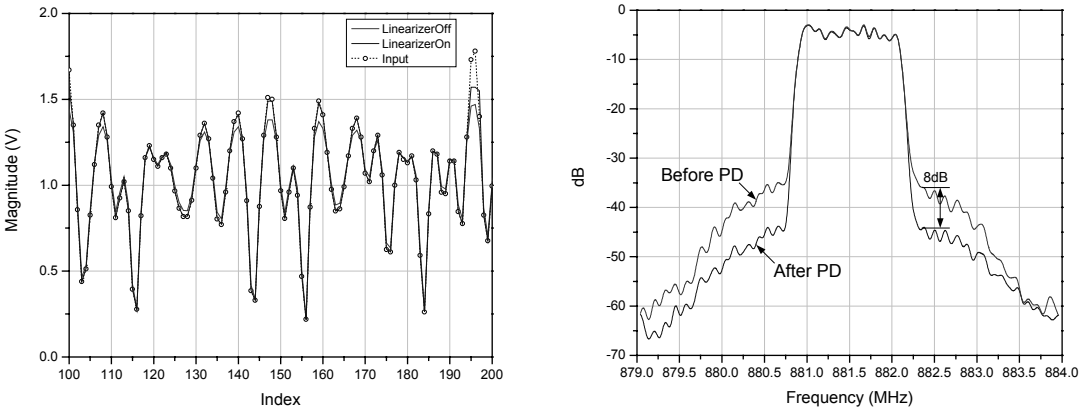


Figure 5.9 Measured group delay of the 0.5W PA (SHF-0189).

Figure 5.10 shows the simulation results from a cdmaOne signal with a bandwidth of 1.2288 MHz. The time-domain signal test shown in Figure 5.10a indicates that the PA output with the linearizer turned on tracks the original input signal well, although the high peak signal is clipped off because of the headroom limitation of the PA. Figure 5.10b shows the spectrum results. The ACPR was measured at 885 kHz offset from the carrier frequency. An ACPR improvement of 8 dB, which was the worst case, was achieved for the cdmaOne 1X signal test at the 3 dB output power backoff from the P_{1dB}.



(a) (b)

Figure 5.10 cdmaOne signal test (BW: 1.2288 MHz, PAPR: 5.7 dB, FB delay: 9 ns, Pout: 24 dBm). (a) Time series. (b) Spectrum.

In Figure 5.11, the ACPR improvement over the output power was investigated. The DDI loop delay of 9 ns caused asymmetry in the ACPR suppression.

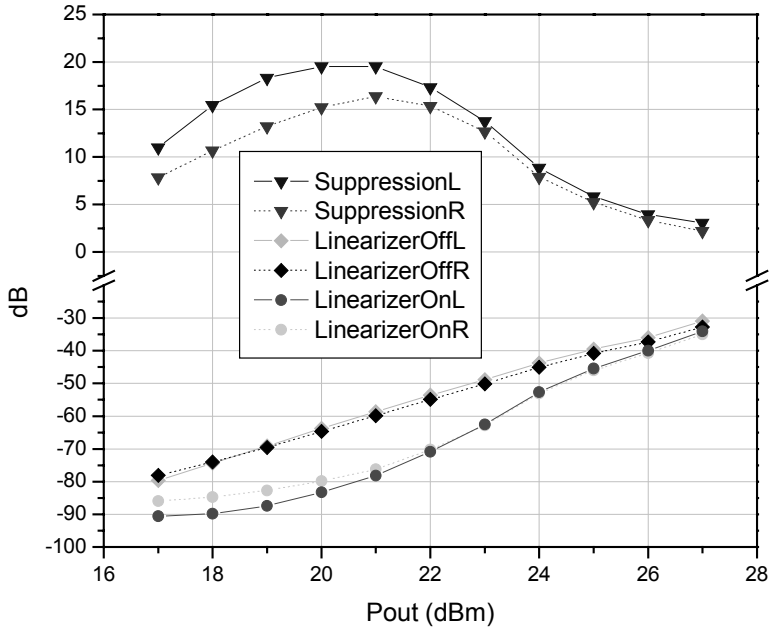


Figure 5.11 Simulated ACPR suppression performance over the output power (FB delay: 9 ns).

However, ACPR improvements of more than 10 dB on both sides were achieved over the output power dynamic range of 6 dB. The output power at the cdmaOne reverse link ACPR spec limit (42 dBc @885 kHz offset) was improved by 1.5 dB from 24 dBm to 25.5 dBm, leading to efficiency enhancement.

Figure 5.12 shows the IMD suppression performance over the loop delay at the output power of 24 dBm using two-tone signals with multiple tone spacings of 1.2288 MHz. For the two-tone signal with a tone spacing of 1.2288 MHz, it shows the IMD3 suppression of more than 17 dB until the FB delay exceeds 9 ns.

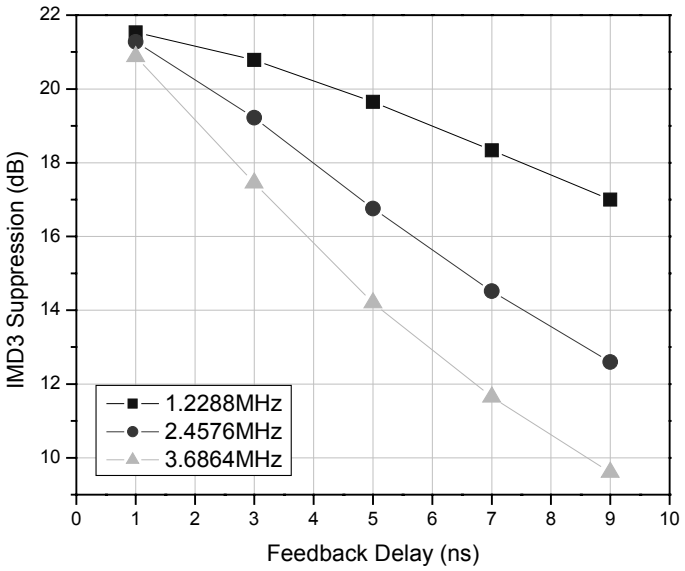
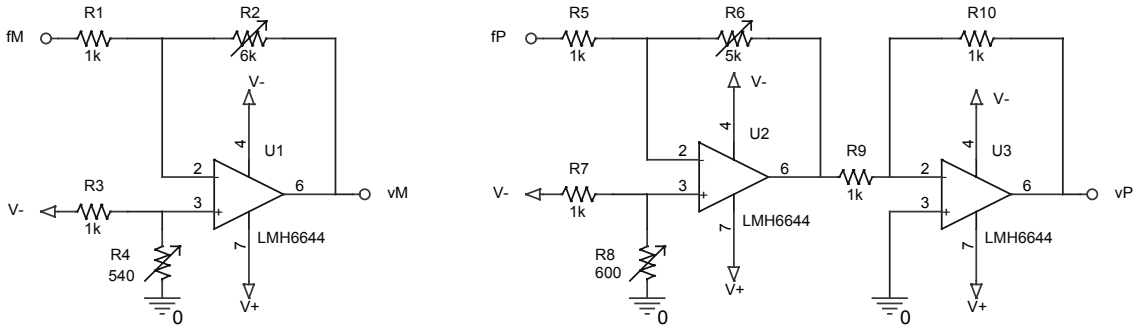


Figure 5.12 IMD3 suppression over the FB delay and tone spacing (Pout: 24 dBm).

5.6 INTERFACING CIRCUIT DESIGN

In the prototype implementation, an interfacing circuit shown in Figure 5.13 was employed

to reduce the discrepancy in the level of the control signal between the gain-phase detector and the vector modulator that consists of the VVA and the VVP. The interfacing circuit was designed to use inverting circuits to gain flexibility in both gain and offset control. Since the VVP is controlled by positive signals, an extra inverting circuit was added, as shown in Figure 5.13b.



(a) (b)

Figure 5.13 Schematics of the interfacing circuit for (a) the VVA control (v_M) and (b) the VVP control (v_P).

The control signals for the VVA, v_M, and the VVP, v_P, can be described respectively as:

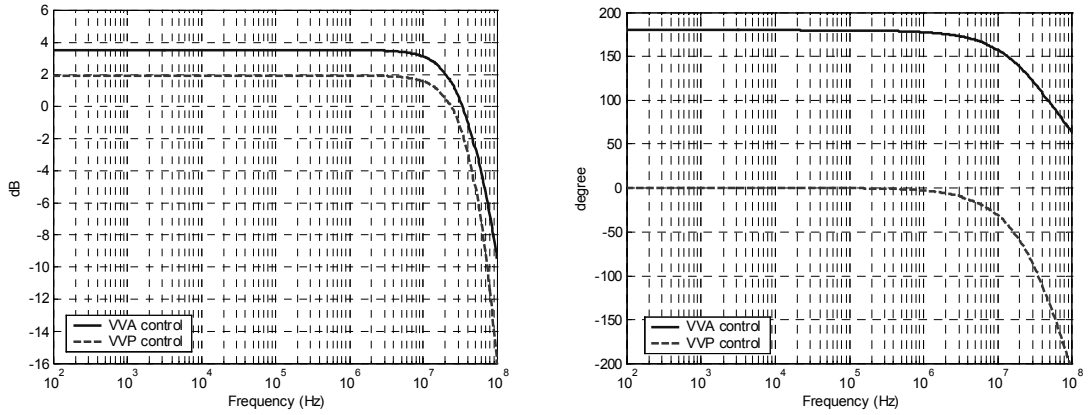
$$v_M = -\left\{ f_M - \left(\frac{G_1 + G_2}{G_3 + G_4} \right) \cdot V_{-} \right\} \cdot \frac{G_1}{G_2}, \tag{5.8}$$

$$v_P = \left\{ f_P - \left(\frac{G_5 + G_6}{G_7 + G_8} \right) \cdot V_{-} \right\} \cdot \frac{G_5}{G_6}, \tag{5.9}$$

where $V\_$ is the negative bias, f_M and f_P are the output of the gain-phase detector, G_i is $1/R_i$, and i is an integer from 1 to 8.

As shown in Figure 5.13, a low-power, high-speed op amp (National Semiconductor LMH6644), which has a slew rate of 130 V/μs under the unit voltage gain, was used in the

design of the interfacing circuit to provide enough operating bandwidth for the interfacing. In the prototype experiment, it displayed total power consumption of 54 mW. Figure 5.14 shows the simulated results of the interfacing circuit in terms of frequency response.



(a) (b)

Figure 5.14 Simulated frequency responses of the interfacing circuit. (a) Magnitude. (b) Phase.

5.7 EXPERIMENTAL RESULTS AND DISCUSSION

Figure 5.15 shows a test system to validate the analog EPD architecture. In the experiments, an arbitrary signal is generated by a signal generator (SG). The PA output is then measured by a spectrum analyzer (SA) and a power meter (PWM). The prototype consists of the vector modulation (VVA and VVP), PA connections, gain and phase error detection, and interface section. The coaxial delay line, which provides a good group delay ripple performance of far less than ±1 ns, was used to compensate for the delay from the PA input to the variable attenuator output. The variable attenuator at the output of the PA was also used to make the small signal PA gain unity.

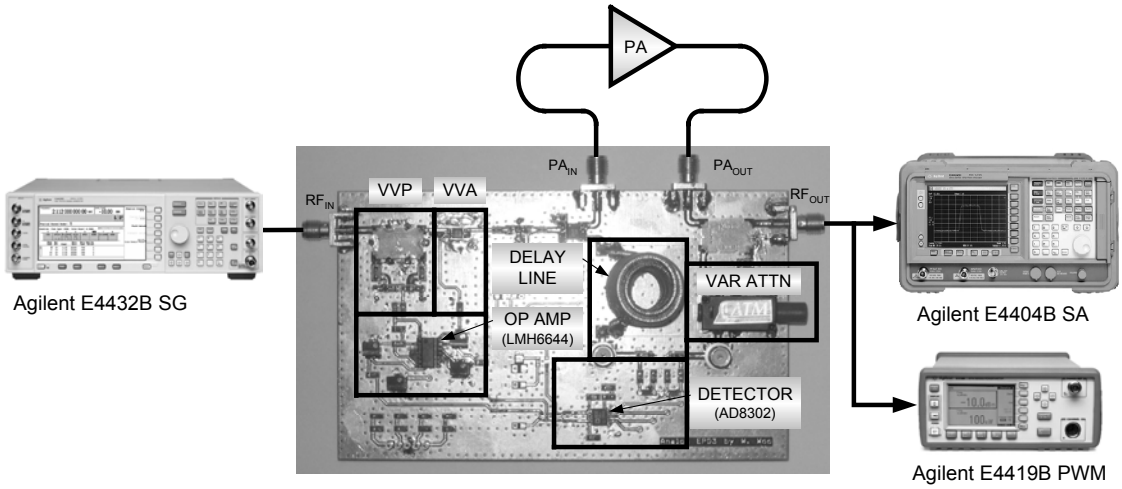
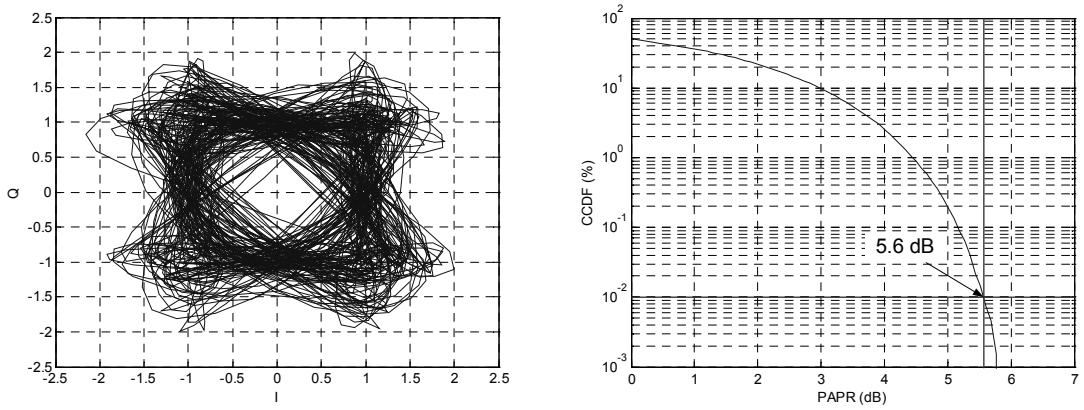


Figure 5.15 Test setup for the analog EPD prototype.

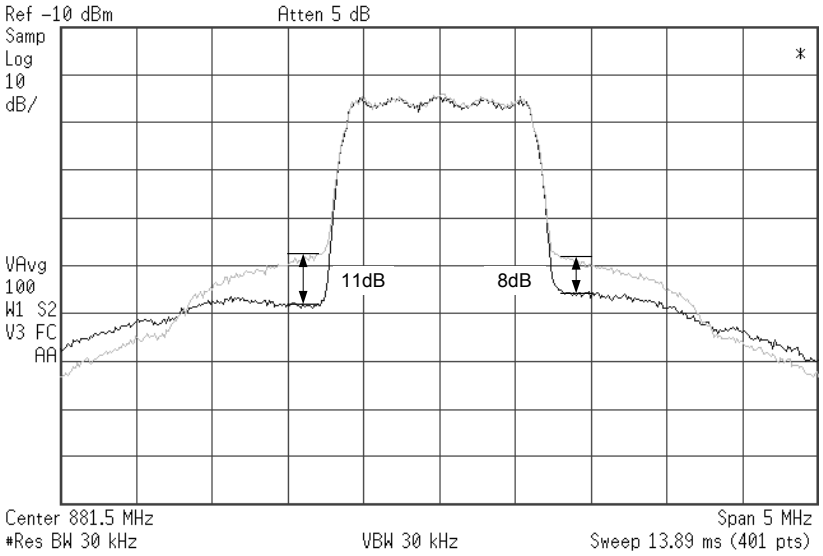
For the experiments, a cdmaOne reverse link signal, which has a 5.6 dB PAPR at 10^{-2}% probability, was used, as shown in Figure 5.16.



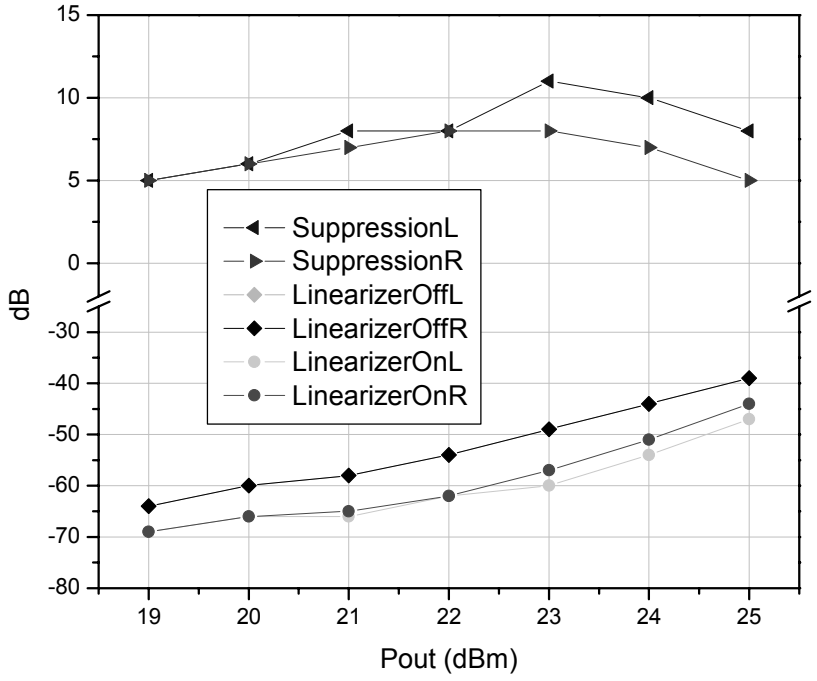
(a) (b)

Figure 5.16 Reverse link cdmaOne signal. (a) Signal trajectory. (b) CCDF.

Figure 5.17 shows the measured results for a 0.5W PA using the reverse link cdmaOne signal, which has a PAPR of 5.6 dB.



(a)

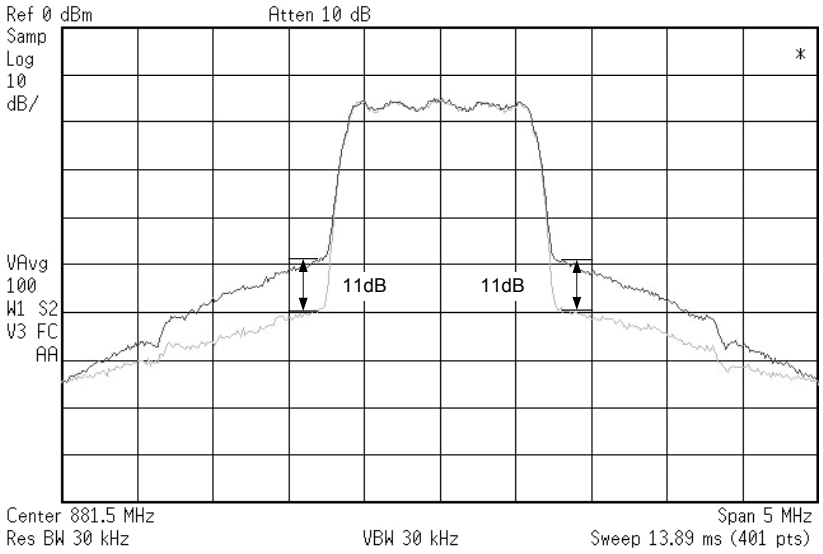


(b)

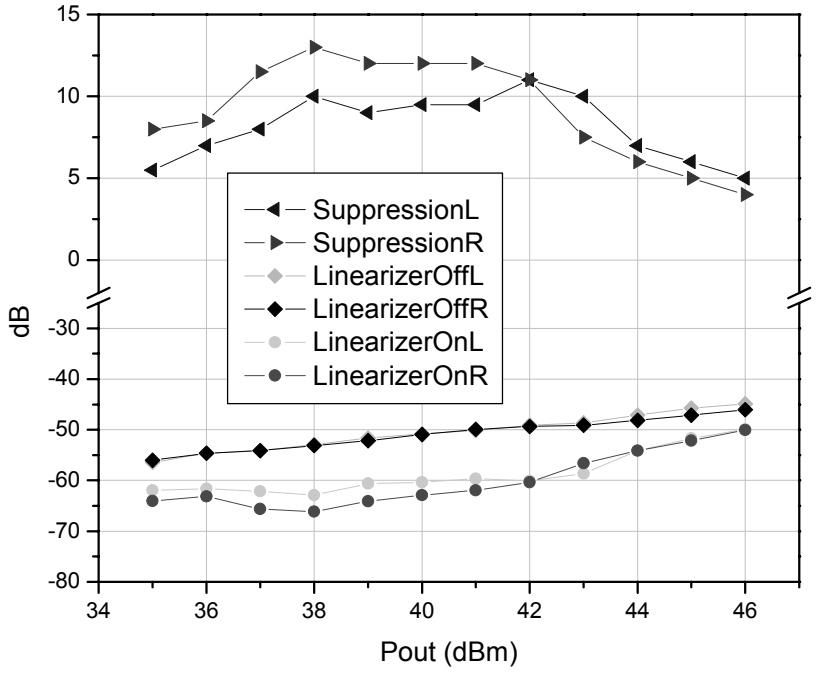
Figure 5.17 Predistortion results (PA: 0.5W SHF-0189, signal: cdmaOne OQPSK reverse link). (a) Spectrum results (Pout: 23 dBm). (b) ACPR improvements vs. output power.

The spectrum results show an ACPR improvement of 11 dB on the left side and of 8 dB on the right side, respectively. However, the degradation in the fifth order region, which is shown in Figure 5.17a, may have several causes, such as the phase shift of the VVA, the intrinsic DDI loop delay, or the non-ideality of the DDI function because of non-ideal PA delay compensation. Figure 5.17b shows the ACPR improvements over the output power. Up to an output power backoff of 2 dB from P_{1dB}, ACPR improvements of 5-11 dB were achieved.

Figure 5.18 shows the measured results for a 90W PA with the same signal as above. The prototype board used in this experiment was improved in terms of VMOD control signal quality by simplifying the interfacing circuit. As shown in Figure 5.18a, the spectrum results display an ACPR improvement of 11 dB at an output power of 42 dBm without degradation in the fifth order region. These results cast doubt on the possibility that degradation in the fifth order region was caused mainly by the non-ideality of the DDI function. Figure 5.18b shows the ACPR improvements over the output power. Until the output power backoff of 4 dB from P_{1dB}, ACPR improvements of 5-13 dB were achieved. It was found from various experiments that the asymmetry of ACPR improvements was caused by the non-ideal PA delay compensation and the intrinsic DDI loop delay. In fact, the intrinsic DDI loop delay cannot be removed. On the other hand, the PA delay compensation can be achieved by using a combination of a coaxial delay line for coarse delay compensation and a lumped L-C delay line for fine delay and delay slope adjustment.



(a)



(b)

Figure 5.18 Predistortion performance (signal: IS-95 OQPSK, PAPR: 5.6 dB, PA: Danam 90W PA). (a) Spectrum results at the output power of 42 dBm. (b) ACPR and efficiency improvements vs. output power.

5.8 CONCLUSION

A new envelope predistortion linearization system that utilizes all analog signal processing was presented. Computer simulation performed using behavioral models indicates the feasibility of our approach. In prototype experiments, the 8-10 dB correction for the 0.5W PA was measured at the output power of 23 dBm, similar to the ADS simulation. Output power at the cdmaOne reverse link ACPR spec limit was improved by 1.3 dB to 25.6 dBm from 24.3 dBm. For the 90W PA, an ACPR improvement of 11 dB was achieved at the output power of 42 dBm. Up to an output power backoff of 4 dB from P_{1dB}, ACPR improvements of 5-13 dB were achieved. The main limitations in predistortion correction are because of: (1) non-ideal vector modulation characteristics, (2) inaccuracies in the gain/phase detector and vector modulator, and (3) group delay in feedback circuits.

CHAPTER VI

ENVELOPE PREDISTORTION FOR POWER AMPLIFIERS WITH MEMORY EFFECTS

This chapter presents an RF envelope predistortion linearization system that uses a combination of an analog envelope predistortion (APD) and a digital LUT-based adaptive envelope predistortion (DPD). The APD system described in Chapter V is used as an inner loop to correct for slowly varying changes in gain, effectively compensating for long-time constant memory effects. The DPD forms the outer loop that corrects the distortion over a wide bandwidth. The APD/DPD combination showed a significant ACPR implement over the DPD alone for a 90W PA.

6.1 INTRODUCTION

Predistortion linearization for RF PAs has attained firm ground in competition with feed-forward linearization systems, obtaining similar IMD suppression with better efficiency and lower cost. However, memory effects in the PA are known as a serious impediment to predistortion linearization [33], [34]. Memory effects cause a hysteresis in the nonlinear transfer characteristics of a PA in response to past inputs. While deterministic, the net effect on the predistortion system is to create an apparent uncertainty in its response, thereby introducing some error in the model used to predistort the nonlinearity. Because they are deterministic processes, memory effects may be modeled

using the Volterra series [37]. Predistorters using a truncated Volterra series may be implemented by the *p*th-order inverse technique [44]. However, the implementation of a *p*th-order inverse system can be very complicated and must be based on a known Volterra series model of the nonlinear channel. Ding *et al*. proposed an adaptive memory polynomial predistorter that only incorporates the terms in the Volterra series that are the dominant distortion mechanisms in RF PAs [53]. It considerably reduced the computational complexity and achieved good predistortion performances for different PA models. However, its implementation is complicated by the additional data required to identify the coefficients associated with the memory effects. Moreover, as the techniques are applied to high-power base station amplifiers operating near compression, increasingly longer delays and higher order polynomials are required to compensate for thermal feedback [33]. Such long delays greatly increase the computational complexity of the predistortion technique, requiring expensive and power hungry high-speed DSP.

In this chapter, a new hybrid digital/analog envelope predistortion architecture for PAs with low-frequency envelope memory effects is presented in conjunction with the experimental results. In Chapters III and VI, a DPD system architecture based on a digital memoryless LUT was described. It provides a precise predistortion for memoryless PAs by using a digitally adaptive LUT architecture. Also, this architecture alleviates some of the computational burden on the DSP and data converters in that the signal manipulation is done directly on the RF signal by using a vector modulator under digital control. The investigations were attempted to incorporate aspects of the memory polynomial DPD as described in [53]. However, the aforementioned issues in its implementation resulted in little improvement over the memoryless architecture, and required considerable hardware

and algorithmic resources. In a separate work, a low-power APD circuit was developed to correct IMD in narrowband RF PAs [60]. While effective, the bandwidth of this technique is inherently limited by delays in the feedback loop. However, it was discovered that the circuit automatically corrects for any gain errors, whether due to static nonlinearities, thermal feedback, or envelope frequency response that are within its loop bandwidth. Thus, it can be used efficiently for compensation for low-frequency envelope memory effects and operate in conjunction with more accurate digital LUT-based architectures.

6.2 Low-frequency Electrical Thermal Feedback Response

The memory effects in RF PAs are known to arise from at least three different sources: (1) RF frequency response, (2) envelope frequency response because of bias circuit interactions, and (3) thermal feedback response [33], [34]. RF frequency response is a short-term memory effect caused by the complex gain variations in the range of instantaneous frequencies of the modulated carrier. While this memory effect may be treated with signal processing, designers developing a feed-forward system, which is also inhibited by this effect, solve the problem by using PAs with flat (linear) frequency response [82]. Given that such feed-forward systems are capable of greater than 30 dB of IMD correction, the author believes that frequency response is not a major inhibitor to the use of predistortion. The dominant source of envelope frequency response comes from the low-frequency response of bias circuits interacting with even order products at baseband frequencies [33]. Like the RF frequency response, this effect may be suppressed with proper bias circuit design [35], [83]. In contrast to RF frequency response and bias effects, thermal feedback that arises from a shift in gain or phase as a result of self-heating cannot

be eliminated easily by correcting device tuning or improving bias circuit response. Moreover, their treatment at the device level may only be achieved by reducing the thermal impedance of the substrate, which requires unnecessarily large device geometries, or by the use of exotic materials. Thermal effects manifest themselves in PA responses to baseband signals of bandwidths up to 1 MHz [33]. This means that, using traditional memory polynomial signal processing methods, a delay of more than 1 μs would be required to deal with such low baseband frequency responses. Therefore, it is desirable to insert an analog subsystem that would compensate for long-time constant effects, leaving the DPD to correct for the high order nonlinearities.

6.3 DIRECT DISTORTION INVERSE PREDISTORTION

One method to treat gain variations is the use of an automatic gain control (AGC) circuit to maintain stable gain averaged over long time periods. Its extension to compensate for phase deviations is straightforward. However, because of the lack of delay compensation in the control loop, the additive feedback used in AGC will necessarily result in instabilities as correction bandwidths are increased. Even if these are suppressed by traditional pole-zero compensation techniques, they inherently introduce other memory effects at high baseband frequencies.

In [84], a more appropriate architecture was suggested to treat long-time constant complex gain errors. This suggested architecture uses a direct inverse approach to multiplicatively correct gain and phase errors. This work presents an analog/digital hybrid implementation of this architecture. Figure 6.1 shows the APD architecture using a direct distortion inverse technique, the details of which were presented in Chapter V.

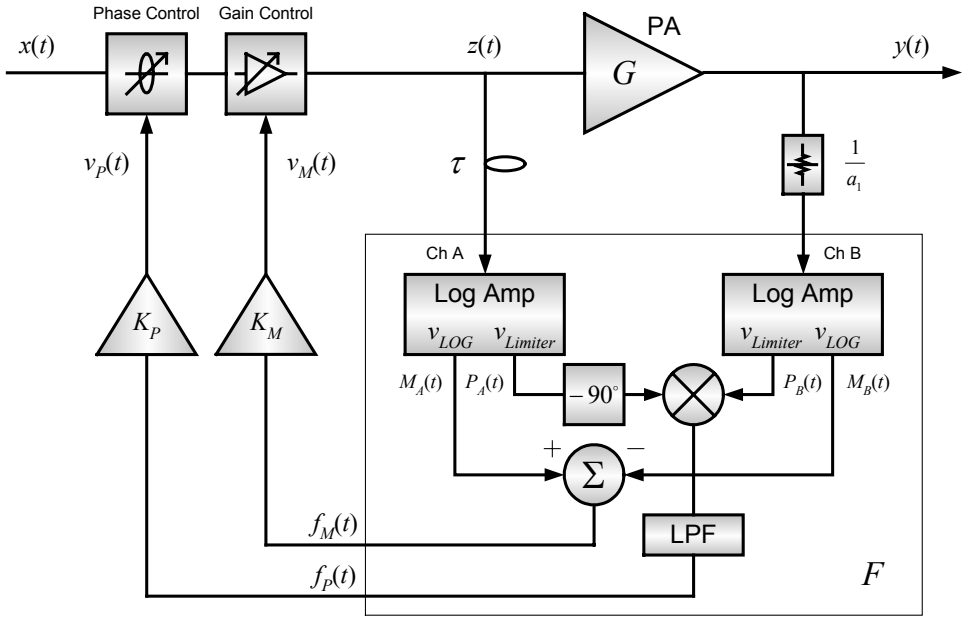


Figure 6.1 Analog envelope predistortion linearization system.

In the APD system, an analog complex gain detector is used to estimate the instantaneous complex gain integrated over some duration that is defined by a low pass filter (LPF). The outputs of the detector are fed back to a VMOD to correct any errors in the gain because of AM-AM or AM-PM distortion. As opposed to conventional analog envelope feedback approaches, this architecture permits some level of predistortion correction, limited only by the accuracy of the analog gain-phase detector and VMOD. It may be shown that the multiplicative feedback employed by the direct distortion inverse architecture is inherently more stable than an AGC system. Therefore, the use of high-order filters, which introduce their own memory effects, is not needed to achieve reasonable bandwidth. This subtle difference in operation between an AGC system and an APD system is what allows the use of APD in conjunction with DPD to compensate for thermal memory effects without the use of complicated memory effect DSP architectures.

6.4 DIGITAL/ANALOG ENVELOPE PREDISTORTION

Figure 6.2 shows the block diagram of the hybrid DPD/APD.

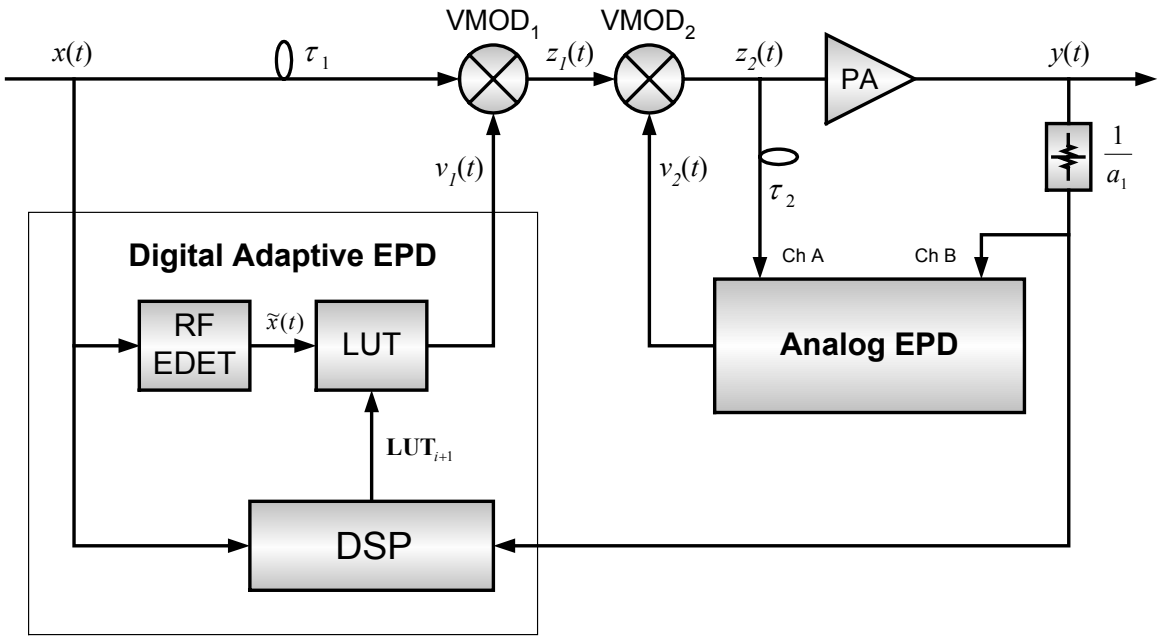


Figure 6.2 Predistortion system using a digital/analog cooperation technique.

In the DPD, a high bandwidth RF EDET extracts the envelope of the input RF signal, which is then used as the index value to the LUT. The modulation signal from the LUT is then multiplied by the delayed input envelope signal in the $VMOD_1$ as a way to suppress the instantaneous distortion at the output of the PA. The delay in the RF signal path is necessary to compensate for the processing and data conversion delay in the LUT-based correction loop.

Adaptation of the LUT is iteratively performed by sampling the signals $x(t)$ and $y(t)/a_1$, demodulating them to obtain the complex envelopes, and using a LMS algorithm to minimize the predistortion function error:

$$\mathbf{LUT}_{i+1} = \mathbf{LUT}_i + \mu \cdot \mathbf{e}_i, \tag{7.1}$$

$$\mathbf{e}_i = 1 - \frac{\mathbf{y}_i}{a_1 \cdot \mathbf{x}_i}, \tag{7.2}$$

where $\mathbf{LUT}_i=[lut_i(0), \cdots, lut_i(S\text{-}1)]^T$, S is the LUT size, μ is the convergence factor, $\mathbf{e}_i=[e_i(0), \cdots, e_i(N\text{-}1)]^T$, $\mathbf{x}_i=[x_i(0), \cdots, x_i(N\text{-}1)]^T$, $\mathbf{y}_i=[y_i(0), \cdots, y_i(N\text{-}1)]^T$, and N is the number of samples.

Using current DSP technology, the convergence rate of the LUT adaptation is too slow to compensate for envelope memory effects with time constants shorter than about 10 ms. While this may improve with successive generations of complementary metal-oxide semiconductor (CMOS) integrated circuit (IC) technology, the costs associated with the additional hardware and the impact on power consumption motivate the use of an analog technique. The APD can be implemented with a commercially available gain-phase detector [79]. The $VMOD_2$ control signal $v_2(t)$, which includes the information of the PA memory effects, is generated from this gain-phase detector. Because of the inherent stability of the APD, no particular attention needs to be paid to its interaction with the DPD.

6.5 Experimental Results and Discussion

The lineup of the PA that was used to validate the performance of the predistortion system consisted of the W-J AH-1 GaAs gain stage, followed by the Motorola MHL9236 LDMOS driver, and the MRF-9085 90W output stage. The last two stages are operated in class-AB mode. The operating frequency is 869-894 MHz, and the total group delay is about 6 ns.

Although linearization performance is often more important than power savings in a base

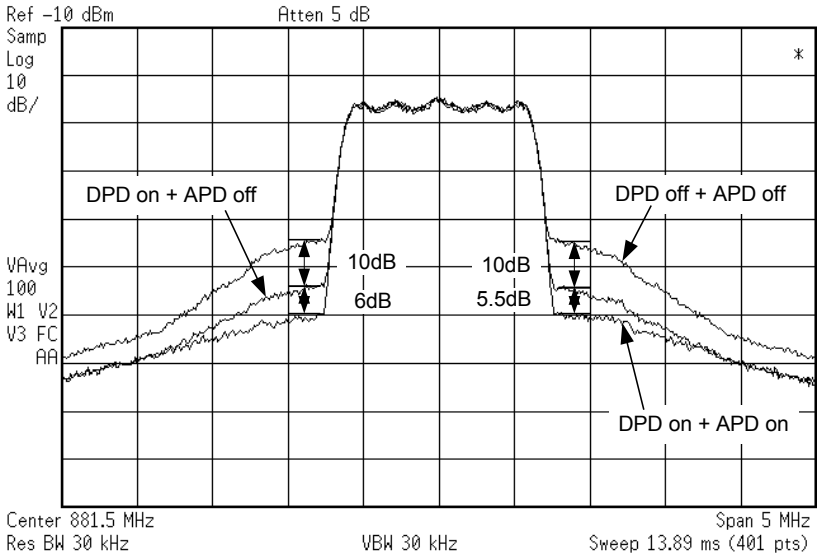
station application, Table 6.1 shows the results for increased output power and efficiency for a given ACPR of –45 dBc at the offsets of 885 kHz for a cdmaOne 1X and 2.15 MHz for a cdmaOne 3X forward link signal.

Table 6.1 Power efficiency improvement

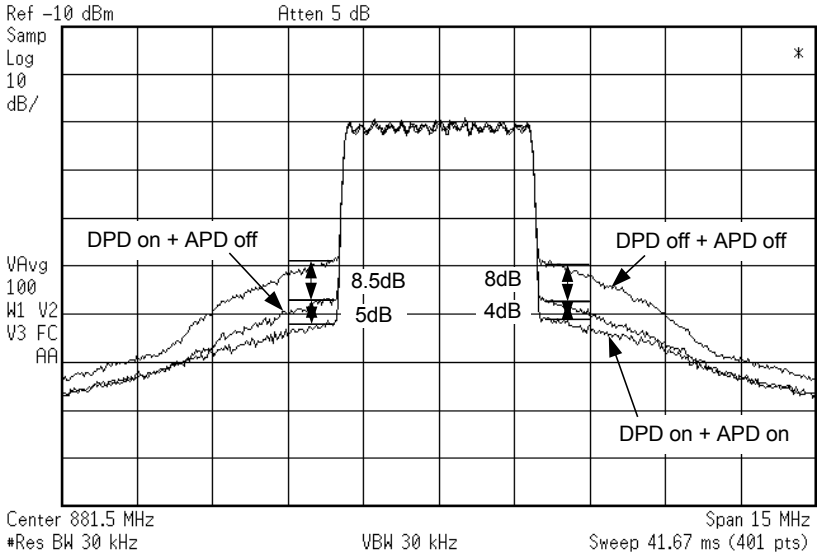
Signal	DPD off + APD off		DPD on + APD off		DPD on + APD on	
	Pout (dBm)	Efficiency (%)	Pout (dBm)	Efficiency (%)	Pout (dBm)	Efficiency (%)
cdmaOne 1X	40.81	10.37	41.94	12.26	42.07	12.51
cdmaOne 3X	40.13	9.28	41.58	11.57	42.01	12.27

The total DC power consumption of the APD section was 104 mW: 50 mW by a gain-phase detector (Analog Device AD8302) to extract the inverse function of the PA nonlinear characteristics and 54 mW by an Op Amp (National Semiconductor LMH6644) to connect the detector to the $VMOD_2$.

Figure 6.3 shows the ACPR improvement results for cdmaOne 1X and 3X signals for the DPD alone, and with the combination of the APD/DPD system.



(a)



(b)

Figure 6.3 Spectrum results for cdmaOne forward link signals at the output power of 40 dBm. (a) cdmaOne 1X (PAPR: 9.6 dB) and (b) cdmaOne 3X (PAPR: 10.5 dB).

Because the impact of low-frequency thermal memory effects increases at higher power, the amount of ACPR improvement afforded by the inclusion of the APD system within the DPD system increased as the power approached 41 dBm, as shown in Figure 6.4.

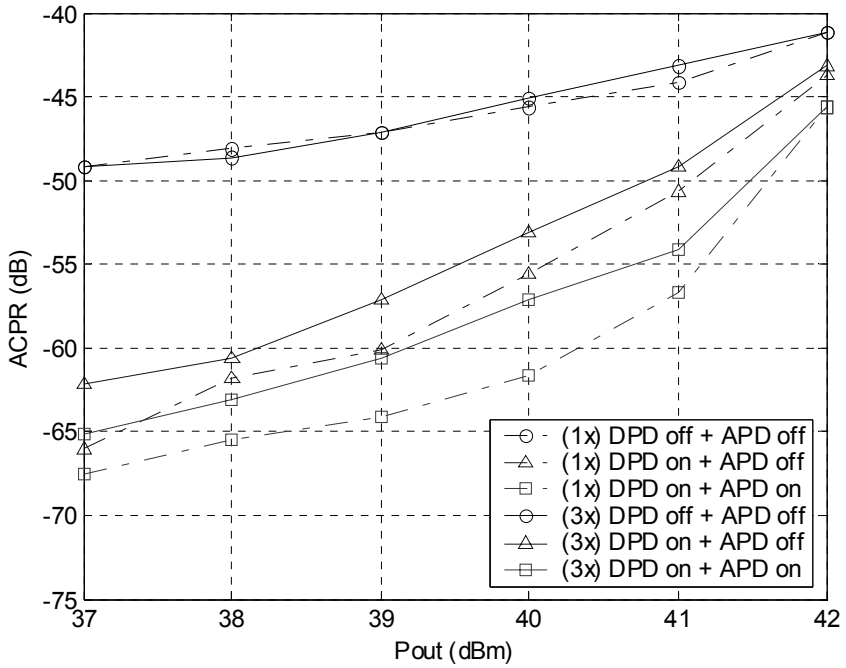


Figure 6.4 ACPR improvement vs. output power for the cdmaOne 1X and 3X forward link signal.

Above 41 dBm, the performance of the system was abruptly reduced because of peak power clipping. Correction performance differed by as much as 1.5 dB between the lower and upper sides of the carrier signal band. Figure 6.4 records worst-case values.

6.6 CONCLUSION

In this chapter, a new digital/analog envelope predistortion linearization system for PAs with low-frequency memory effects was discussed. A digital LUT-based adaptive predistortion system was used to compensate for instantaneous distortion owed to the memoryless portion of the PA nonlinear transfer characteristic. An analog envelope predistortion system, implemented with commercially available components, was inserted

to compensate for long-time constant envelope memory effects. The resulting combination considerably decreases the computational complexity load of the digital system and significantly improves linearity and efficiency at high power levels.

CHAPTER VII

CONCLUSIONS

7.1 SUMMARY AND PRINCIPLE CONCLUSIONS

The research presented in this dissertation proceeded from two primary motivations. The first is that RF PAs are one of main components in wireless communication system, but are intrinsically nonlinear in transfer characteristics. The second motivation is that PA memory effects impede the use of predistortion as a commercially competitive technique for other PA linearization.

This dissertation considered various techniques for predistortion linearization of RF PAs: baseband digitally adaptive predistortion, hybrid digital/RF envelope predistortion for PAs with small memory effects, analog envelope predistortion using the direct distortion inverse technique, and combinational digital/analog predistortion for PAs with low envelope frequency memory effects. This includes mixed-signal system simulation techniques in conjunction with the behavioral modeling of analog and digital components. Also, the prototype implementation details of the proposed architectures were included in this dissertation.

Chapter 1 gave the principal motivations for the work presented in this dissertation. Also, PA linearization techniques and the identification and compensation techniques of

PA memory effects were briefly outlined. A dissertation outline and a list of contributions were given.

In Chapter 2, a digital adaptation technique based on error vector minimization of received PA output waveforms was developed. In conjunction with the adaptation technique, an adaptive baseband-to-baseband test system for the characterization of RF PAs and for the validation of linearization algorithms was also implemented. Using this system, algorithms for memoryless baseband digital predistortion may be tested in automated fashion, simulating the performance of a real-time DSP processor operating in conjunction with commercially available RF PAs.

In Chapter 3, a mixed-signal behavioral simulation system for RF PA predistortion was developed using the Agilent ADS^{TM} computer-aided design system. Behavioral models were extracted from the RF components and simulated in the same file with the digital components. A digital look-up table was employed for adaptation. Trade-offs were made between digital design and RF component designs to optimize the performance of the system. The predistortion system performed linearization for a physical model of a PA by using the dynamic feedback of the difference between input and output envelope signals to adaptively compensate for the gain and phase distortion. The simulation system yielded various design factors for system optimization.

In Chapter 4, a wideband adaptive predistortion linearization system for PAs with small memory effects was developed based on a high-speed RF envelope modulation that is applied to the input signal of an amplifier. By controlling the VMOD based on the RF envelope level, the PA is linearized to the extent that memoryless predistortion is possible. The performance of the envelope predistortion system was examined for a 0.5W GaAs

HFET and a 90W PEP LDMOS PA using multi-tone and CDMA signals. A wideband multi-tone test showed IMD suppressions of 12 dB over a 25 MHz BW eight-tone continuously phase modulated signal for the 0.5W PA and the same improvement over an 18 MHz BW for the 90W PA. Using the CDMA signal, more than 17 dB and 12 dB correction in ACPR was achieved for the 0.5W PA and the 90W PA, respectively.

In Chapter 5, a new envelope predistortion linearization system that uses all analog signal processing was developed for low-power applications. Computer simulations performed using behavioral models indicate the feasibility of the approach. Based on the simulation results, a prototype of the architecture was implemented. The linearization performances for a 0.5W GaAs HFET and a 90W PEP LDMOS PA were examined in prototype experiments. The 8-10 dB correction for the 0.5W SHF-0189 PA was achieved at an output power of 23 dBm, similar to the ADS^{TM} simulation. The output power at the cdmaOne reverse link ACPR spec limit was improved by 1.3 dB to 25.6 dBm from 24.3 dBm. For the 90W PA, an ACPR improvement of 11 dB was achieved at the output power of 42 dBm. Until the output power backoff of 4 dB, ACPR improvements of 5-13 dB were achieved. Main limitations in the predistortion system were because of: (1) non-ideal vector modulation characteristics, (2) inaccuracies in the gain/phase detector and vector modulator, and (3) group delay in feedback circuits.

In Chapter 6, a new digital/analog envelope predistortion linearization system for PAs with low-frequency memory effects was developed. A digital LUT-based adaptive predistortion system was used to compensate for instantaneous distortion caused by the memoryless portion of the PA nonlinear transfer characteristic. An analog envelope predistortion system, implemented with commercially available components, was inserted

to compensate for long-time constant envelope memory effects. The resulting combination considerably decreases the computational complexity load of the digital system and significantly improves linearity and efficiency at high power levels.

7.2 SUGGESTIONS FOR FUTURE WORK

The work carried out in this dissertation has generated areas for possible future study. Some suggested extensions and additions are in the following discussion. In the development of the hybrid digital/RF envelope predistortion system, the system correction bandwidth was limited by the LUT-based correction-loop subsystem as well as by the intrinsic memory effects of a PA. Wideband signal handling capability of the correction-loop subsystem depends heavily on the linear VMOD control capability over the frequency range of interest. Because DAC outputs to control the VMOD show *sinc* function effects in the frequency domain because of the limitation of the reconstruction sampling rate, a future investigation would focus on the insertion of a reconstruction filter with an *inverse-sinc* response between the DAC and the VMOD with a goal of making the resultant frequency responses flat over the range. Also, the delay compensation required in the correction-loop subsystem was achieved by a coaxial delay line, which displays a small amount of group delay ripple (±1 ns), but has a large volume and weight. Although a surface acoustic wave (SAW) delay line approach may be a possible alternative, reduction of the large group delay ripple warrants further attention.

Enhancing the performance of the analog envelope predistortion system presents several opportunities for additional investigation. Among such opportunities are improved design of low-power circuits, better performing VVA and VVP circuit designs, increases in

frequency range and bandwidth, reduction of the group delay in the gain/phase detector and the interface section, reduction of glitch phenomena at low envelope power levels because of the log amp-based detectors, and finally monolithic integration of this architecture.

APPENDIX

DESIGN RESOURCES

A.1 FPGA LUT DESIGN

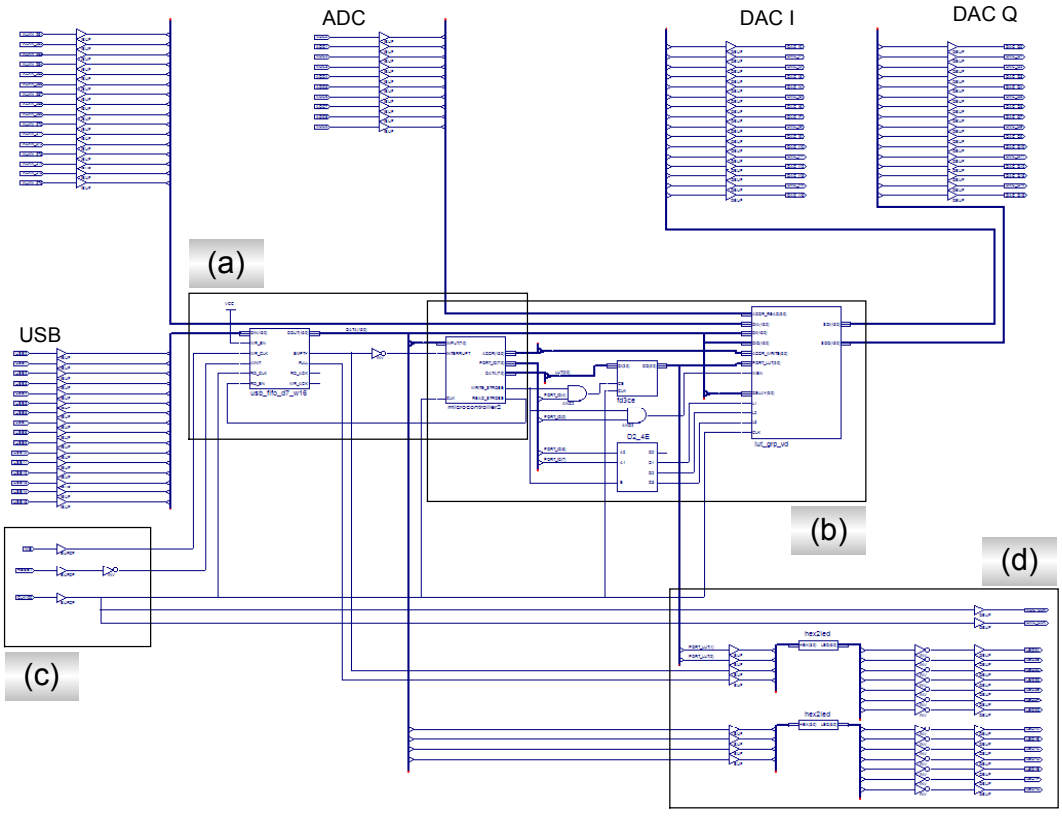


Figure A.1 Top-level of the FPGA LUT design.

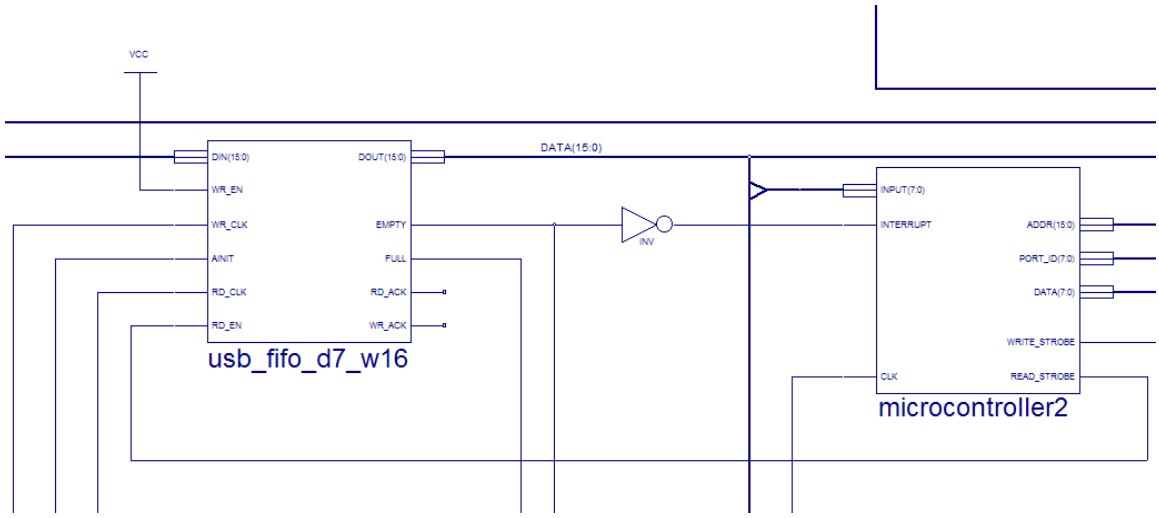


Figure A.2 Enlarged figure of the area (a).

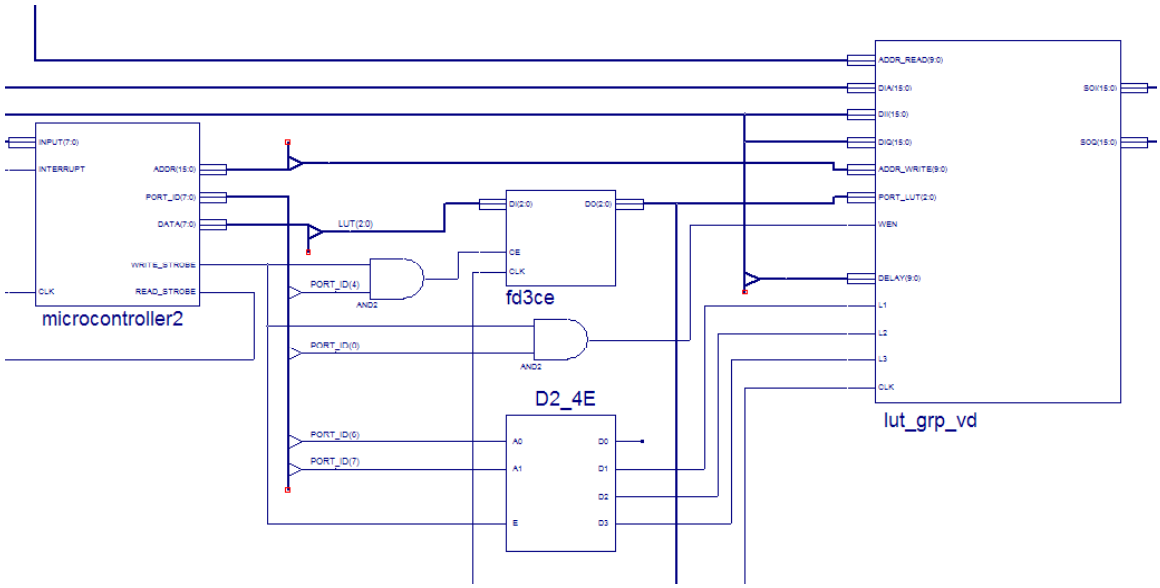


Figure A.3 Enlarged figure of the area (b).

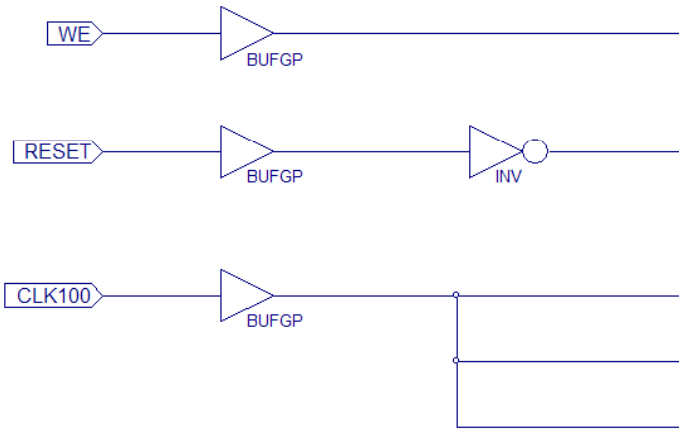


Figure A.4 Enlarged figure of the area (c).

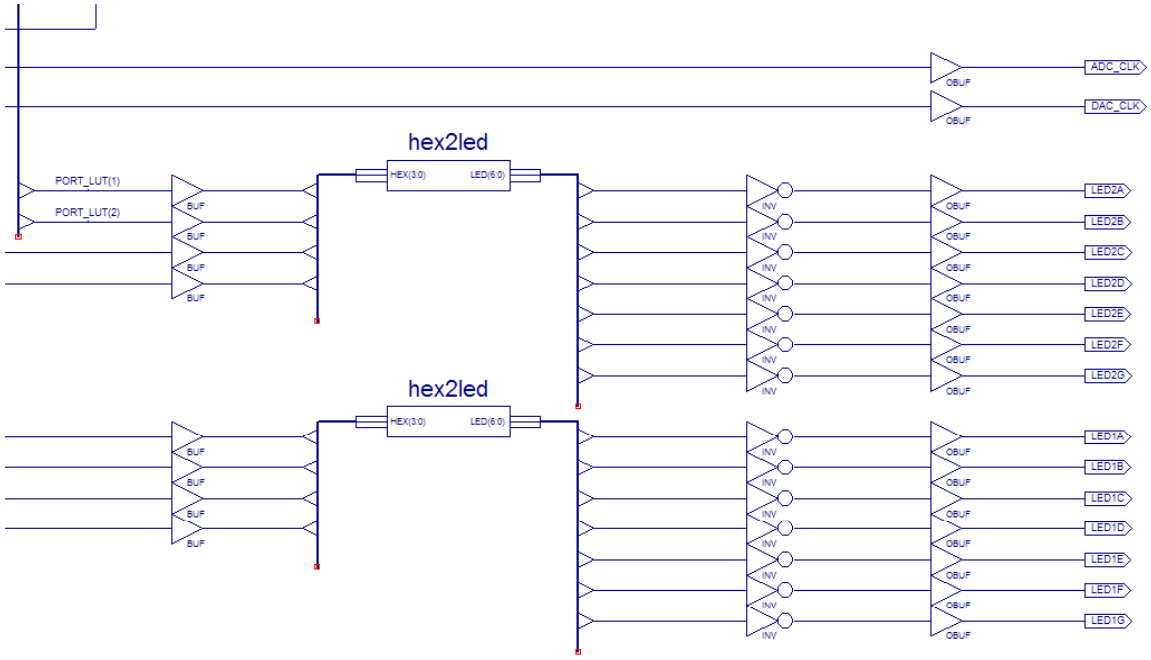


Figure A.5 Enlarged figure of the area (d).

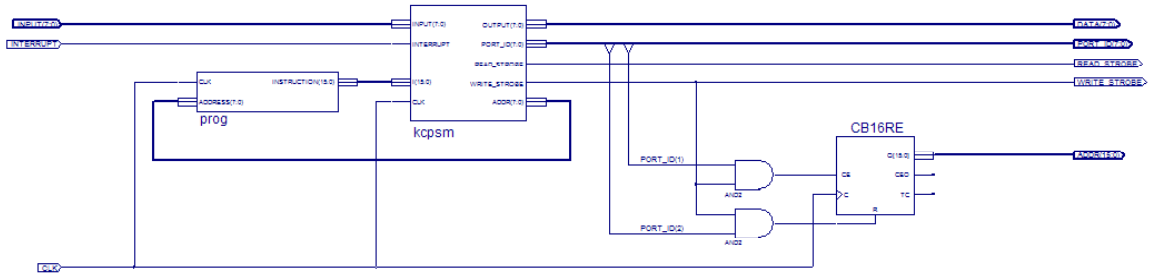


Figure A.6 Microcontroller.

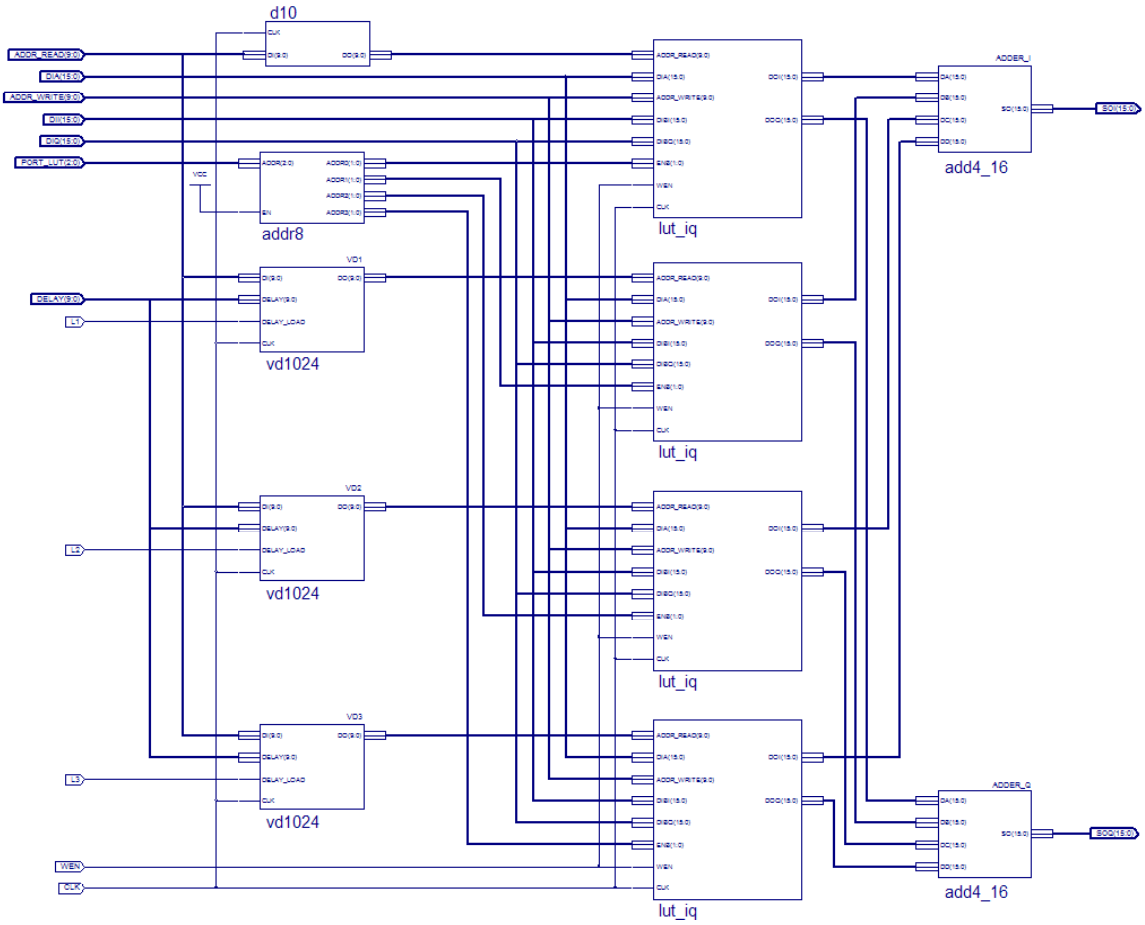


Figure A.7 LUT group.

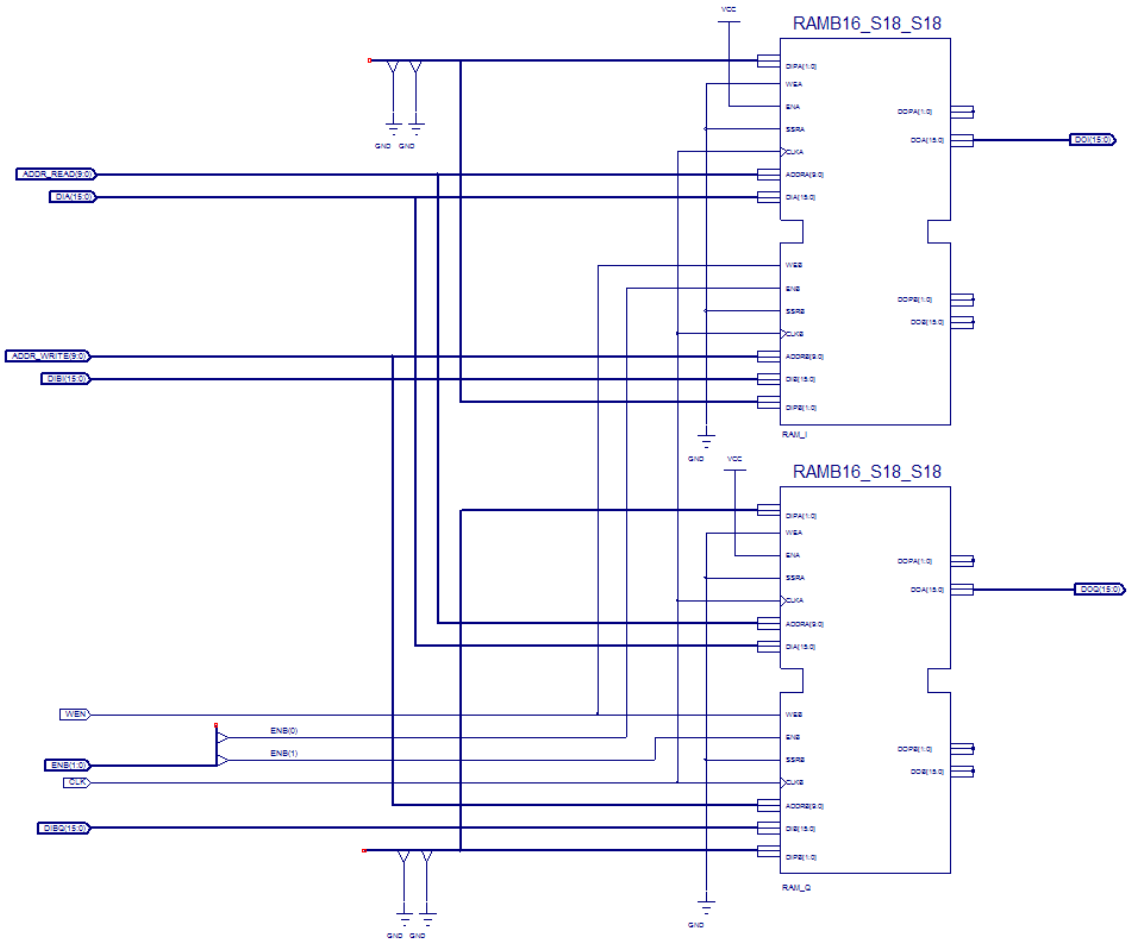


Figure A.8 LUTiq.

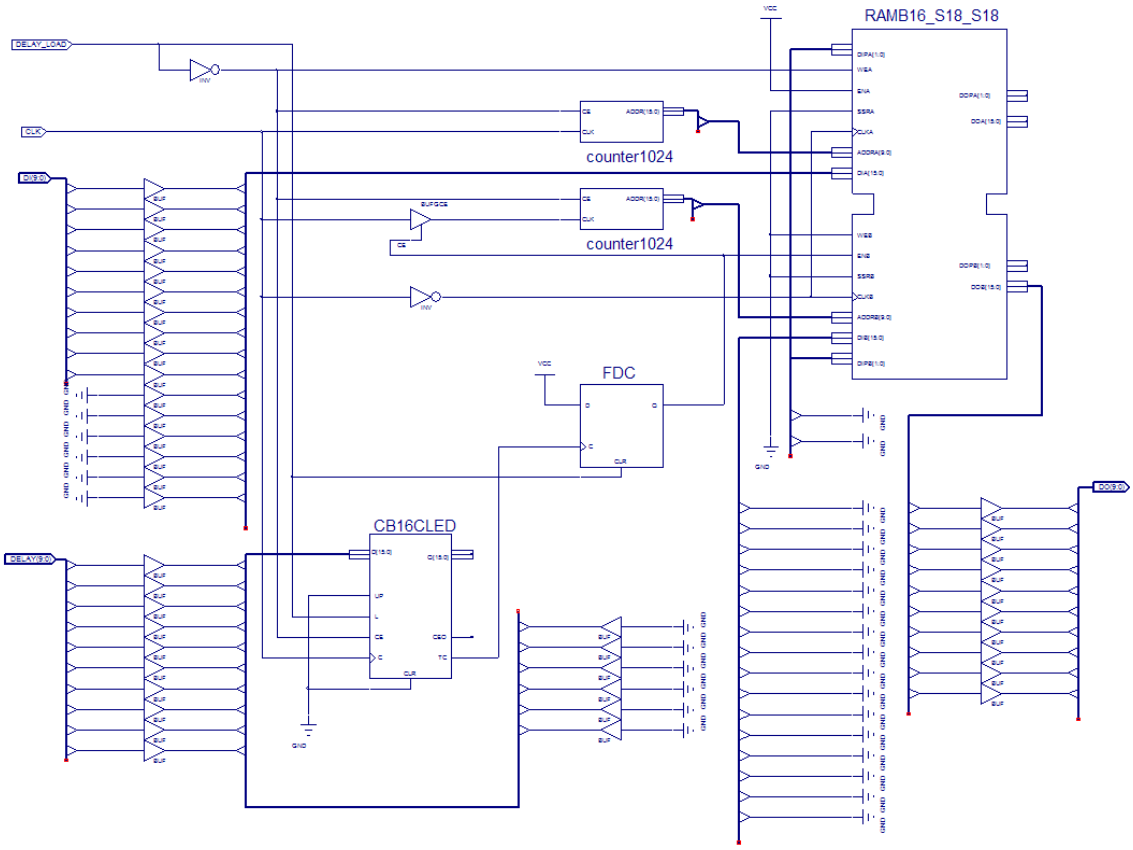


Figure A.9 VD1024.

A.2 ANALOG-BASED RF ENVELOPE PREDISTORTION SYSTEM

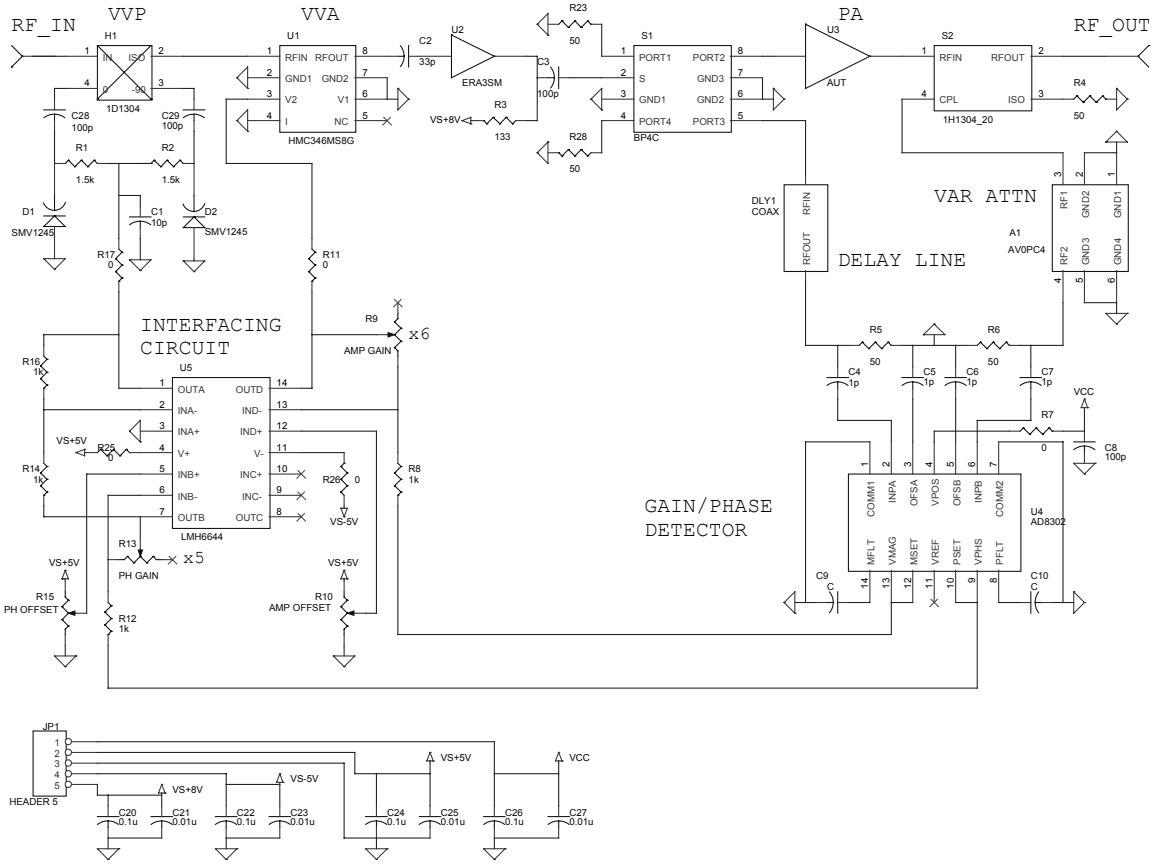


Figure A.10 Analog-based EPD circuit.

REFERENCES

[1] P. B. Kenington, *High-Linearity RF Amplifier Design*, Boston, MA: Artech House, 2000.

[2] J. S. Kenney and A. Leke, "Design Considerations for Multicarrier CDMA Base Station Power Amplifiers," *Microwave J.*, vol. 42, no. 2, pp. 76-84, Feb. 1999.

[3] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, Boston, MA: Artech House, 1999.

[4] H. S. Black, "Stabilised Feedback Amplifiers," *The Bell system Technical J.*, vol. 13. no. 1, pp. 1-18, Jan. 1934.

[5] H. S. Black, "*Wave Translation System*," U.S. Patent 2,102,671, filed 22 Apr. 1932, granted 21 Dec. 1937.

[6] C. Hsieh and E. Strid, "A S-Band High Power Feedback Amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1977, pp. 182-184.

[7] S. D. Roy and D. Sinha, "An Active Feedback Block and Its Applications," *IEEE Trans. Audio and Electroacoust.*, vol. 19, no. 3, pp. 256-258, September 1971.

[8] T. Nesimoglu, C. N. Canagarajah, and J. P. McGeehan, "An Active Feedback for Wideband Amplifier Linearization," in *Proc. IEEE Int. 3G Mobile Commun. Technol. Conf.*, March 2000, pp. 112-116.

[9] T. Arthanayake and H. B. Wood, "Linear Amplification Using Envelope Feedback," *IEE Electron. Lett.*, vol. 7, no. 7, pp. 145-146, April 1971.

[10] J. Cardinal and F. M. Ghannouchi, "A New Adaptive Double Envelope Feedback (ADEF) Linearizer for Solid State Power Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 7, pp. 1508-1515, July 1995.

[11] M. Johansson and T. Mattsson, "Transmitter Linearization Using Cartesian Feedback for Linear TDMA Modulation," in *Proc. IEEE Veh. Technol. Conf.*, May 1991, pp. 439-444.

[12] H. S. Black, "*Translating System,*" U.S. Patent 1,686,792, filed 3 Feb. 1925, granted 9 Oct. 1928.

[13] H. Seidel, H. R. Beurrier, and A. N. Friedman, "Error Controlled High Power Linear Amplifiers at VHF," *The Bell System Technical J.*, vol. 47, pp. 651-722, May/June 1968.

[14] J. K. Cavers, "Adaptation Behavior of a Feedforward Amplifier Linearizer," *IEEE Trans. Veh. Technol.*, vol. 44, no. 1, pp. 31-40, Feb. 1995.

[15] S. Narahashi and T. Nojima, "Extremely Low-Distortion Multi-Carrier Amplifier-Self-Adjusting Feed-Forward (SAFF) Amplifier," in *Proc. IEEE Int. Conf. Commun.*, vol. 3, June 1991, pp. 1485-1490.

[16] M. G. Choi, Y. C. Jeong, and I. H. Park, "*Method and Apparatus for Amplifying Feedforward Linear Power Using Pilot Tone Hopping*," US Patent No. 6,081,156, 2000.

[17] R. H. Bauman, "*Adaptive Feedforward System*," US Patent No. 4,389,618, 1983.

[18] Y. Yang, Y. Kim, J. Yi, J. Nam, B. Kim, W. Kang, and S. Kim, "Digital Controlled Adaptive Feedforward Amplifier for IMT-2000 Band," in *IEEE MTT-S Int. Microwave Symp. Dig*., vol. 3, June 2000, pp. 1487-1490.

[19] M. G. Overmann and J. F. Long, "*Feedforward Distortion Minimization Circuit*," US Patent No. 5,077,532, 1991.

[20] M. D. Benedetto and P. Mandarini, "A New Analog Predistortion Criterion with Application to High Efficiency Digital Radio Links," *IEEE Trans. Microwave Theory Tech.*, vol.43, no.12, pp. 2966-2974, Dec. 1995.

[21] J. Yi, Y. Yang, M. Park, W. Kang, and B. Kim, "Analog Predistortion Linearizer for High-Power RF Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 48, no. 12, pp. 2709-2713, Dec. 2000.

[22] Y. Kim, I. Chang, and Y. Jeong, "An Analog Predistortion Linearizer Design," *Microwave J.*, vol. 48, no. 2, pp. 118-126, Feb. 2005.

[23] J. Han, T. Chung, and S. Nam, "Adaptive Predistorter for Power Amplifier Based on Real-Time Estimation of Envelope Transfer Characteristics," *Electron. Lett.*, vol. 35, no. 25, pp. 2167-2168, Dec. 1999.

[24] A. Springer, A. Gerdenitsch, and Z. Li, "Adaptive Predistortion for Amplifier Linearization for UMTS Terminals," in *IEEE Int. Symp. Spread-Spectrum Tech. & Appl. Dig.*, Sep. 2002, pp. 78-82.

[25] L. Ding, G. T. Zhou, D. R. Morgan, M. Zhengxiang, J. S. Kenney, J. Kim, and C. R. Giardina, "A Robust Digital Baseband Predistorter Constructed Using Memory Polynomials," *IEEE Trans. Communications*, vol. 52, no. 1, pp. 159-165, Jan. 2004.

[26] C. Turner, "Calculation of TMS320LC54x Power Dissipation," *in Texas Instruments application report SPRA164*, June 1997.

[27] C. G. Rey, "Adaptive Polar Work-Function Predistortion," *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 6, pp. 722-726, June 1999.

[28] E. G. Jeckeln, F. Beauregard, M. A. Sawan, and F. M. Ghannouchi, "Adaptive Baseband/RF Predistorter for Power Amplifiers Through Instantaneous AM-AM and AM-PM Characterization using Digital Receivers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, May 2000, pp. 489-492.

[29] S. Kusunoki, K. Yamamoto, T. Hatsugai, K. Tagami, H. Nagaoka, N. Tominaga, K. Osawa, K. Tanabe, S. Sakurai and T. Iida, "Power Amplifier Module with Digital Adaptive Predistortion for Cellular Phone," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, June 2002, pp. 765-768.

[30] C. Gentzler and Z. Regev, "*Amplifier Linearization by Learned Linear Behavior*," US Patent 6,369,344, May 28, 2002.

[31] W. Bösch and G. Gatti, "Measurement and Simulation of Memory Effects in Predistortion Linearizers*," IEEE Trans. Microwave Theory Tech*., vol. 37, no. 12, pp. 1885-1890, Dec. 1989.

[32] J. Vuolevi, T. Rahkonen, and J. Manninen, "Measurement Technique for Characterizing Memory Effects in RF Power Amplifiers," *IEEE Trans. Microwave Theory Tech*, vol. 49, no. 8, pp. 1383-1389, Aug. 2001.

[33] J. Vuolevi and T. Rahkonen, *Distortion in RF Power Amplifiers*, Norwood, MA: Artech House, 2003.

[34] J. S. Kenney, W. Woo, M. D. McKinley, H. Ku, and Y. C. Park, "Practical Limitations of Predistortion Linearization Systems for RF Power Amplifiers," in *Proc. Asia-Pacific Microwave Conf.*, Nov. 2003, FE1-1.

[35] A. Rabany, L. Nguyen, and D. Rice, "Memory Effect Reduction for LDMOS Bias Circuits," *Microwave J.*, vol. 46, no. 2, Feb. 2003.

[36] V. Volterra, "Sopra Le Funzioni che Dipendono de Altre Funzioni," *Rend. R. Accademia dei Lincei 2° Sem*, pp. 97-105, 141-146, 153-158, 1887.

[37] S. A. Mass, *Nonlinear Microwave and RF Circuits*, Norwood, MA: Artech House, 2003.

[38] N. Wiener, *Response of a Nonlinear Device to Noise*, Report No. 129, Radiation Laboratory, M.I.T., Cambridge Mass., Apr. 1942.

[39] M. Schetzen, *The Volterra and Wiener Theories of Nonlinear Systems*, Reprint Edition, Malabar, FL:Krieger, 1989.

[40] M. Schetzen, "Measurement of the Kernels of a Nonlinear System of Finite Order," *Int. J. of Control*, vol. 1(3), pp. 251-263, Mar. 1965; *Corrigendum*, vol. 2(4), pp.408, Oct. 1965.

[41] N. Wiener, *Nonlinear Problems in Random Theory*, The Technology Press of MIT and John Wiley and Sons, 1958.

[42] Y. W. Lee and M. Schetzen, "Measurement of the Wiener Kernels of a Non-Linear System by Cross-Correlation," *Int. J. of Control*, vol. 2, pp. 237-254, 1965.

[43] M. Schetzen, "A Theory of Non-Linear System Identification," *Int. J. of Control*, vol. 20, no. 4, pp. 577-592, 1974.

[44] M. Schetzen, "Theory of *p*-th Order Inverses of Nonlinear Systems," *IEEE Trans. Circuits and Systems*, vol. CAS-23, no. 5, pp. 285-291, May 1976.

[45] K. Narendra and P. Gallman, "An Iterative Method for the Identification of Nonlinear Systems Using a Hammerstein Model," *IEEE Trans. Automatic Control*, vol. 11, no. 3, pp. 546-550, July 1966.

[46] C. J. Clark, G. Chrisikos, M. S. Muha, A. A. Moulthrop, and C. P. Silva, "Time-Domain Envelope Measurement Technique with Application to Wideband Power Amplifier Modeling," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 12, pp. 2531-2540, Dec. 1998.

[47] H. Ku, M. D. McKinley, and J. S. Kenney, "Extraction of Accurate Behavior Models for Power Amplifiers with Memory Effects Using Two-Tone Measurements," in *IEEE MTT-S Int. Microwave Sym. Dig*., vol. 1, June 2002, pp. 139-142.

[48] J. Kim and K. Konstantinou, "Digital Predistortion of Wideband Signals Based on Power Amplifier Model with Memory," *Electron. Lett.*, vol. 37, no. 23, pp. 1417-1418, Nov. 2001.

[49] D. M. Etter and Y. Cheng, "System Modeling Using an Adaptive Delay Filter," *IEEE Trans. Circuits and Systems*, vol. CAS-34, no. 7, pp. 770-774, July 1987.

[50] H. Ku and J. S. Kenney, "Behavioral Modeling of Nonlinear RF Power Amplifiers Considering Memory Effects," *IEEE Trans. Microwave Theory Tech.*, vol. 51, no. 12, Dec. 2003.

[51] W. Shan, L. Sundstrom, and B. Shi, "Spectral Sensitivity of Predistortion Linearizer Architectures to Filter Ripple," in *Proc. IEEE Veh. Technol. conf.*, vol. 3, Oct 2001, pp. 1570-1574.

[52] C. Eun and E. J. Powers, "A New Volterra Predistorter Based on the Indirect Learning Architecture," *IEEE Trans. Signal Processing*, vol. 45, no. 1, pp. 223-227, Jan. 1997.

[53] L. Ding, G. T. Zhou, D. R. Morgan, Z. Ma, J. S. Kenney, J. Kim, C. R. Giardina, "Memory Polynomial Predistortion Based on the Indirect Learning Architecture," in *Proc. IEEE Global Telecomm. Conf.*, vol. 1, Nov. 2002, pp. 967-971.

[54] W. Woo and J. S. Kenney, "A Predistortion Linearization System for High Power Amplifiers with Low Frequency Envelope Memory Effects," to appear in *IEEE Int. Microwave Symp. Dig.*, June 2005.

[55] W. Woo, L. Ding, J. S. Kenney, and G. T. Zhou, " An RF/DSP Test Bed for Baseband Pre-Distortion of RF Power Amplifiers," in *Proc. the 57th ARFTG Conf.*, May 2001, pp. 54-70.

[56] W. Woo, E. Park, K. U-yen, and J. S. Kenney, "Mixed-Signal Behavioral Simulation of an Envelope Predistortion Linearization System for RF Power Amplifiers," in *Proc. IEEE Behavioral Modeling and Systems Workshop*, Oct. 2002, pp. 67-70.

[57] W. Woo, E. Park, K. U-yen, and J. S. Kenney, "Wideband Predistortion Linearization System for RF Power Amplifiers Using an Envelope Modulation Technique," in *Proc. IEEE Radio and Wireless Conf.*, Aug. 2003, pp. 401-404.

[58] W. Woo, M. Miller, and J. S. Kenney, "Predistortion Linearization System for High Power Amplifiers," in *IEEE Int. Microwave Symp. Dig.*, June 2004, pp. 677-680.

[59] W. Woo, M. Miller, and J. S. Kenney, "A Hybrid Digital/RF Envelope Predistortion Linearization System for Power Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 1, Jan. 2005.

[60] W. Woo and J. S. Kenney, "A New Envelope Predistortion Linearization Architecture for Handset Power Amplifiers," in *Proc. IEEE Radio and Wireless Conf.*, Sep. 2004, pp. 175-178.

[61] J. K. Cavers, "A Linearizing Predistorter with Fast Adaptation," in *Proc.* 40th *IEEE Veh. Technol. Conf.*, 1990, pp. 41-47.

[62] K. Voelker, "Apply error vector measurements in communications design", *Microwave & RF*, pp.143-152, Dec. 1995.

[63] M. S. Heutmaker, "The Error Vector and Power Amplifier Distortion," in *Proc. IEEE Wireless Commun. Conf.*, 1997, pp. 100-104.

[64] "Using Error Vector Magnitude Measurements to Analyze and Troubleshoot Vector-Modulate Signals," *Agilent Product Note* 89400-14.

[65] Y. Park, W. Woo, R. Raich, J. S. Kenney, and G. T. Zhou, "Adaptive Predistortion Linearization of RF Power Amplifiers Using Lookup Tables Generated from Subsampled Data," in *Proc. IEEE Radio and Wireless Conf.*, Aug. 2002, pp. 233-236.

[66] W. Woo and J. S. Kenney, "Mixed-signal simulation of a power amplifier predistortion linearization system," *the 58th ARFTG Conf.*, San Diego, pp. 101-109, November 2001.

[67] J. S. Kenney and A. Leke, "Power amplifier spectral regrowth for digital cellular and PCS applications," *Microwave Journal,* Vol. 38, No. 10, pp. 74-92, October 1995.

[68] A. Leke and J. S. Kenney, "Behavioral Modeling of Narrowband Microwave Power Amplifiers with Applications in Simulating Spectral Regrowth," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1385-1388, June 17-21, 1996.

[69] R. H. Walden, "Analog-to-Digital Converter Survey and Analysis," *IEEE J. Select. Areas Commun.*, vol. 17, no. 4, pp. 539-550, Apr. 1999.

[70] J. S. Kenney, W. Woo, M. D. McKinley, H. Ku, and Y. C. Park, "Practical Limitations of Predistortion Linearization Systems for RF Power Amplifiers," in *Proc. Asia-Pacific Microwave Conf*, Nov. 2003.

[71] W. Woo, M. Miller, and J. S. Kenney, "Predistortion Linearization System for High Power Amplifiers," in *2004 IEEE MTT-S Int. Microwave Symp. Dig.*, June 2004, pp. 677-680.

[72] W. Woo, M. Miller, and J. S. Kenney, "A Hybrid Digital/RF Envelope Predistortion Linearization System for Power Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 1, Jan. 2005.

[73] J. K. Cavers, "Optimum Table Spacing in Predistorting Amplifier Linearizers," *IEEE Trans. Microwave Theory Tech.*, vol. 48, no. 5, pp. 1699-1705, Sep. 1999.

[74] B. Razavi, *RF Microelectronics*, New Jersey: Prentice Hall PTR, 1998.

[75] Y. Park, W. Woo, R. Raich, J. S. Kenney, and G. T. Zhou, "Adaptive Predistortion Linearization of RF Power Amplifiers Using Lookup Tables Generated from Subsampled Data," in *Proc. IEEE Radio and Wireless Conf.*, Aug. 2002, pp. 233-236.

[76] J. Cowles and B. Gilbert, "Accurate Gain/Phase Measurement at Radio Frequencies up to 2.5 GHz," *Analog Dialogue* 35-05, 2001.

[77] F. Ellinger, R. Vogt, and W. Bächtold, "Compact reflective-type phase-shifter MMIC for C-band using a lumped element coupler," *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 5, pp. 913-917, May 2001.

[78] C. Rapp, "Effects of HPA-Nonlinearity on a 4-DPSK/OFDM-Signal for a Digitial Sound Broadcasting System," in *Proc. the Second European Conf. on Satellite Communications, Liege, Belgium*, Oct. 1991, pp. 179-184.

[79] *Datasheets for the RF/IF gain and phase detector* (*AD8302*), Analog Devices. Available: http://www.analog.com.

[80] W. Kang, I. Chang, and M. Kang, "Reflection-Type Low-Phase-Shift Attenuator," *IEEE Trans. Microwave Theory Tech*., vol. 46, no. 7, pp. 1019-1021, July 1998.

[81] R. N. Hardin, E. J. Downey, and J. Munushian, "Electronically Variable Phase Shifters Utilizing Variable Capacitance Diodes," in *Proc. IRE*, vol. 48, May 1960, pp. 944-945.

[82] J. S. Kenney and S. A. Avis, "The Relationship between IMD and ACPR," *Wireless Design and Development*, pp. 7-8, Sep. 2000.

[83] J. F. Sevic, K. L. Burger, and M. B. Steer, "A Novel Envelope-Termination Load-Pull Method for ACPR Optimization of RF/Microwave Power Amplifiers," in *IEEE int. Microwave Symp. Dig*., vol. 2, June 1998, pp. 723-726.

[84] E. G. Jeckeln, F. M. Ghanouchi, and M. A. Sawan, "A New Adaptive Predistortion Technique Using Software-Defined Radio and DSP Technologies Suitable for Base Station 3G Power Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 52, no. 9, pp. 2139-2147, Sep. 2004.

VITA

Wangmyong Woo was born in Kyunggi, Korea, in 1971. He received the B.S. degree in computer engineering in 1998 from the Myong Ji University, Yongin, Korea, and the M.S. degree in electrical and computer engineering in 2000 from the Georgia Institute of Technology, Atlanta, GA. Since 2000, he has been working toward the Ph.D. degree in electrical and computer engineering at the Georgia Institute of Technology.

His research interests include RF, analog, mixed-signal circuits and systems, FPGA design, embedded system design, RF power amplifier linearization, and wireless communication systems.